

MODEL NAME : *ANREDB4100*
PCB NO : *LA-G441P*
BOM P/N : *431ACQ31L**

Dell/Compal Confidential

Schematic Document

(Spyglass Whiskey Lake U)

BOM Structure

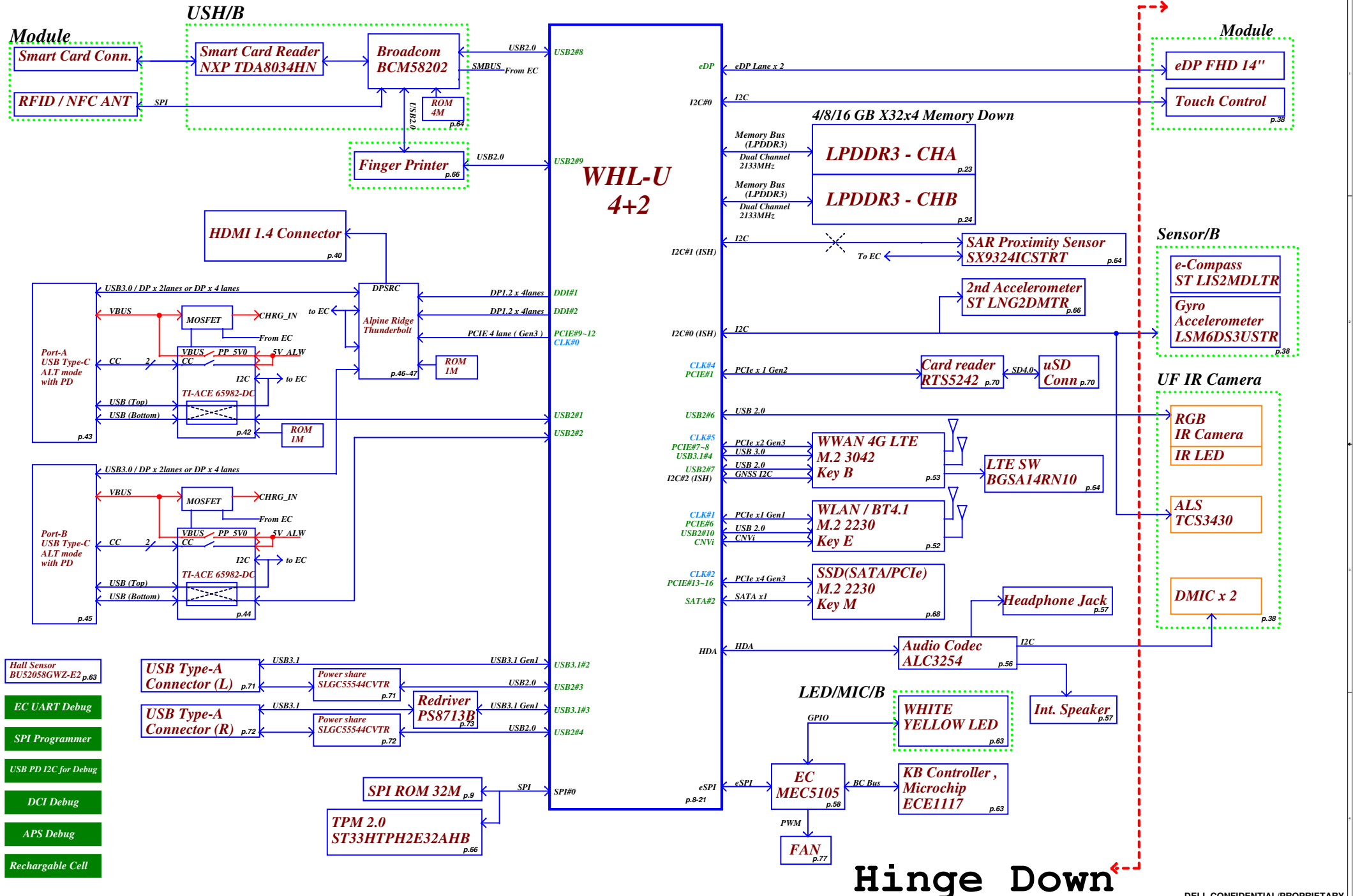
- 128M@ : 128M SPI ROM
- 256M@ : 256M SPI ROM
- @ : Nopop Component
- RF@ : RF Component
- @RF@ : RF Nopop Component
- EMC@ : EMI Component
- @EMC@ : EMI Nopop Component
- 5105@ : Option for MEC5105
- 5106@ : Option for MEC5106
- ST@ : ST TPM
- 750@ : Nuvoton TPM
- NRTD3@ : non RTD3 support
- RTD3@ : RTD3 support
- NDS3@ : non Deep sleep support
- DS3@ : Deep sleep support
- XDP@ : XDP Component
- DB@ : Debug Component
- BreakDown@ : Breakdown Component

2018-09-28

Rev: 1.0 (A00)

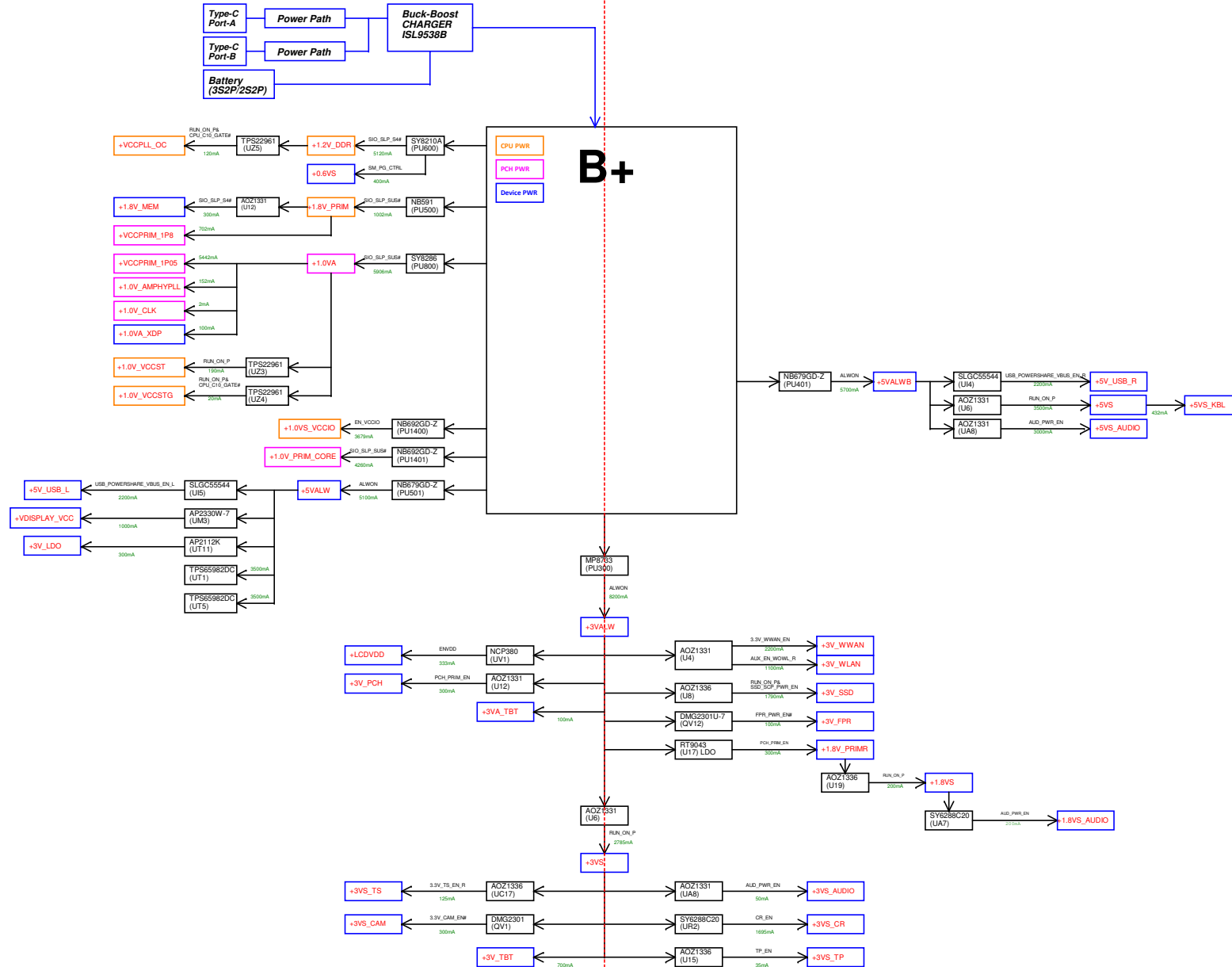
PVT

Hinge up



Left Side

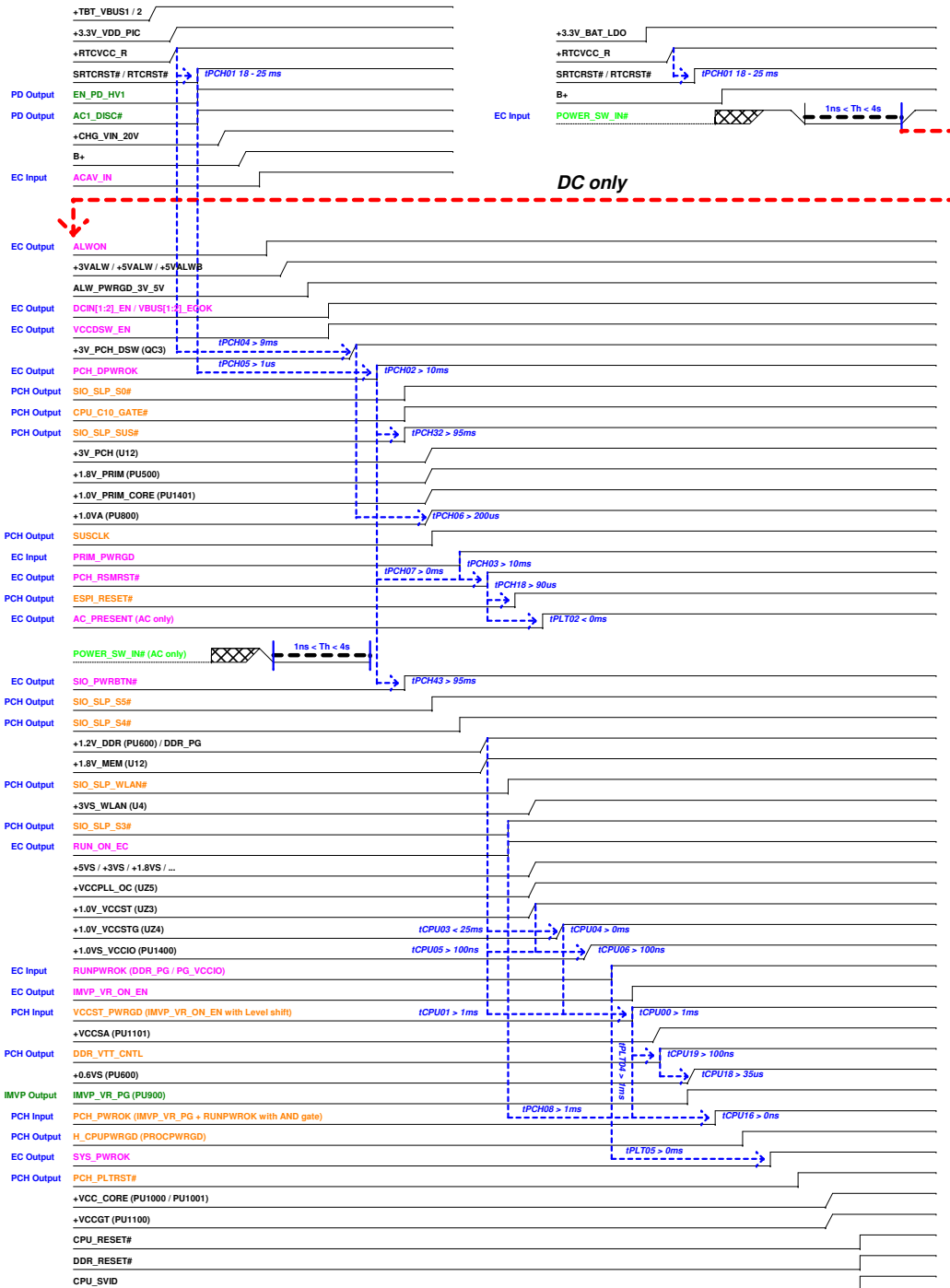
Right Side



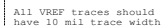
Support Deep Sleep

[AC in] (remove RTC)

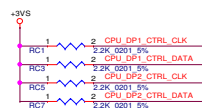
[Battery only, AC absent] (remove RTC)



Security Classification Issued Date: 2018/01/23 Compal Secret Data Designated Date: 2022/12/31				DELL CONFIDENTIAL/PROPRIETARY <i>Compal Electronics, Inc.</i>	
Title: P005 - Power Sequence				Rev: 1/2008	
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MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date: 2018/01/23 Drawn: Checked: of 100	



COMPENSATION PU FOR eDP
CAD Note:
Trace width=5 mils
Isolation Spacing=25mil,
Max length=100 mils.

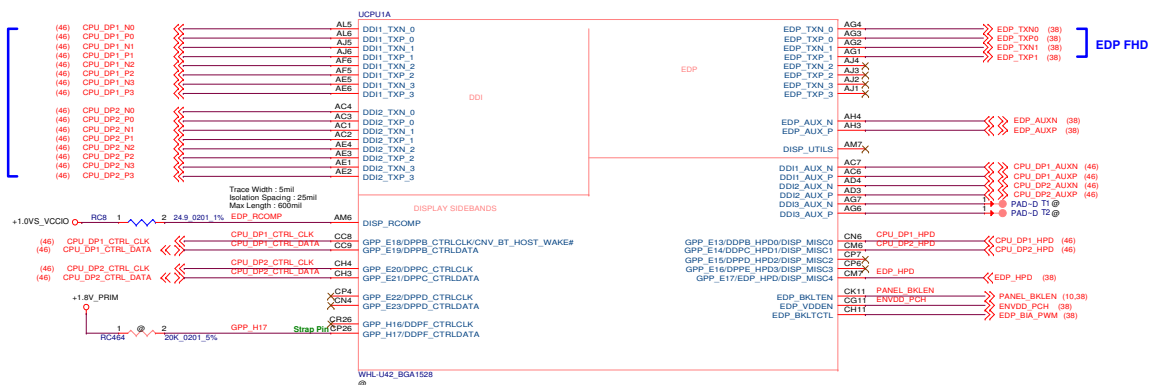


Alpine Ridge

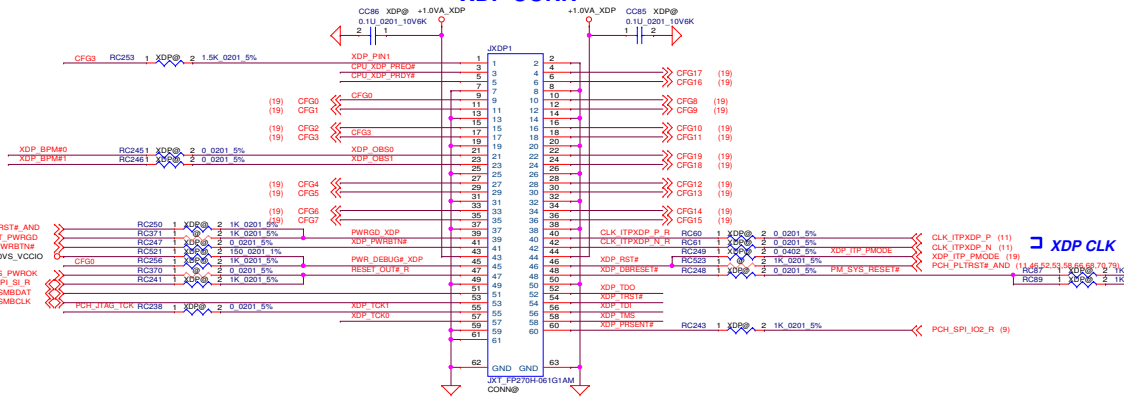
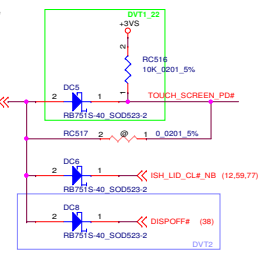
GPP_E19 (WEAK INTERNAL PD)
 0 = Port B is not detected. (Default)
 1 = Port B is detected.

GPP_E21 (WEAK INTERNAL PD)
 0 = Port C is not detected. (Default)
 1 = Port C is detected.

GPP_E23 (WEAK INTERNAL PD)
 0 = Port D is not detected. (Default)
 1 = Port D is detected.

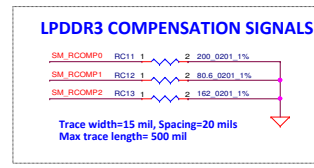
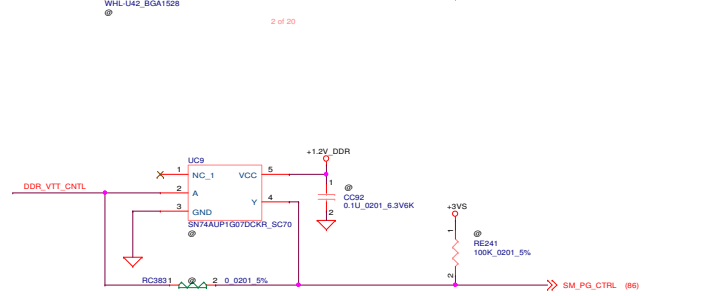
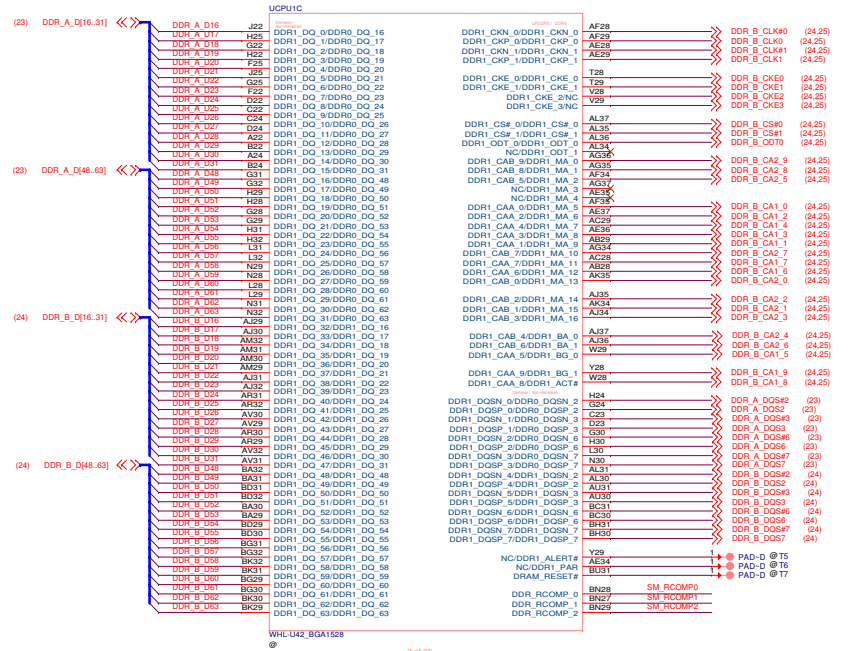
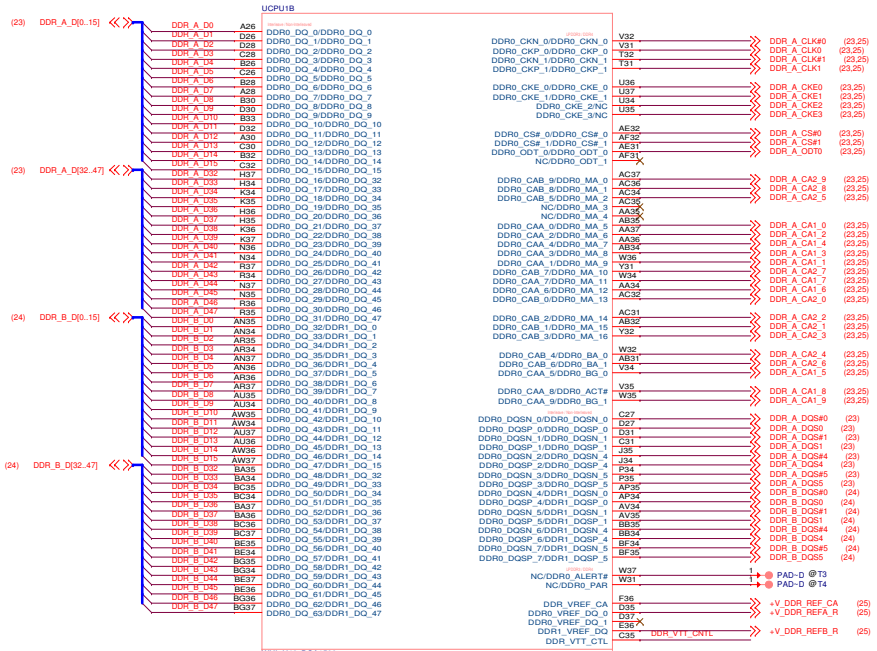


PCH GLITCH ISSUE MITIGATION(PDG p.130)



Security Classification		Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY Compal Electronics, Inc.	
Issued Date	2015/12/16	Deciphered Date	2016/12/13	Title	P007 - WHL-U(2/14)MISC.XDP
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				Sheet	7 of 100

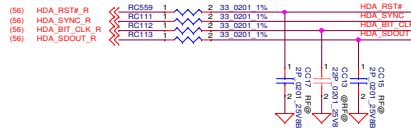
LPDDR3, Ballout for side by side(Non-Interleave)



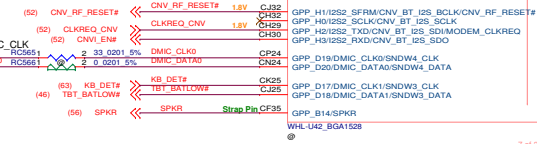
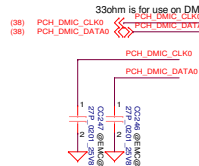
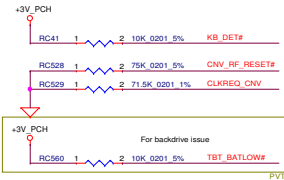
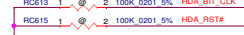
Capacitor to only be used for HDA_SDO, HDA_RST#, and HDA_SDI for EMI purposes and should be a close as possible to the PCH.
For HDA_SDO and HDA_RST# the cap should be after the series resistor closest to the PCH.

HDA for AUDIO

close to PCH



PCH GLITCH ISSUE MITIGATION(PDG p.130)



TOP SWAP OVERRIDE

GPP_B14 / SPKR (WEAK INTERNAL PD)

0 = Disable Top Swap mode. (Default)

1 = Enable Top Swap mode.

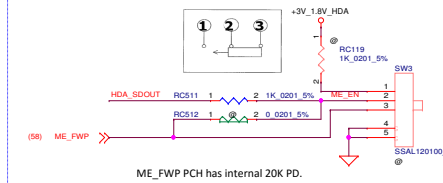


Flash Descriptor Security Override

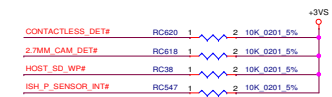
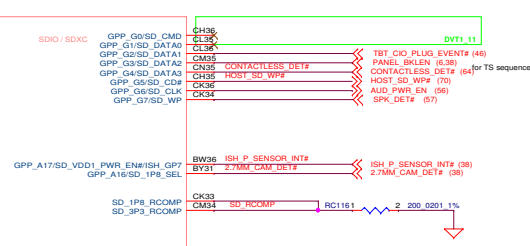
HDA_SDO / I2S0_TXD (WEAK INTERNAL PD)

Disable ME Protect (ME can be updated) ----> Pin1 & Pin2 short

Enable ME Protect (ME cannot be updated)--> Pin3 & Pin2 short(Default position)

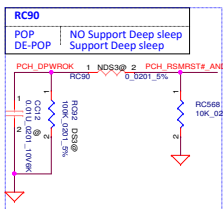
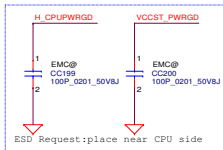
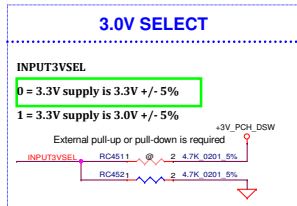
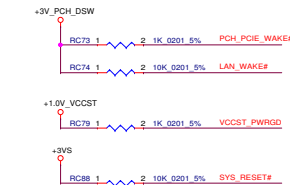
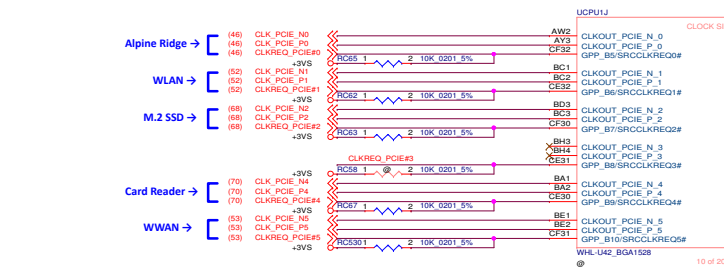


ME_FWP PCH has internal 20K PD.

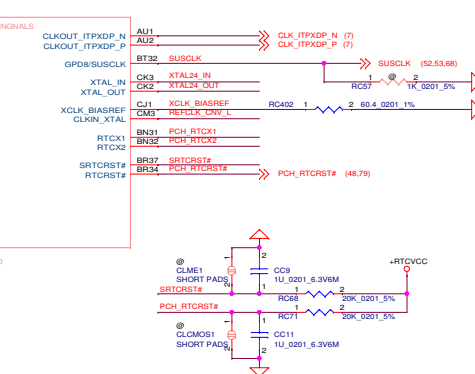
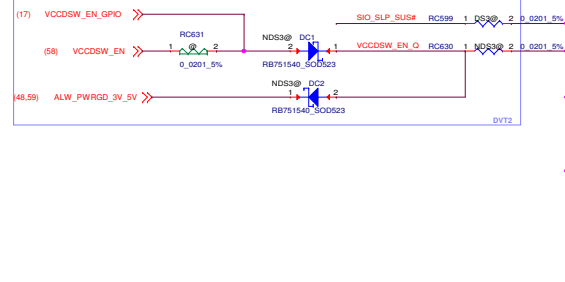
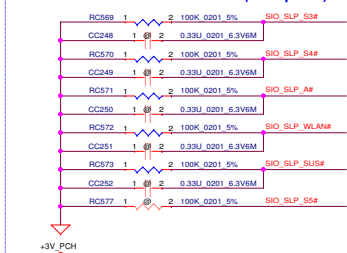


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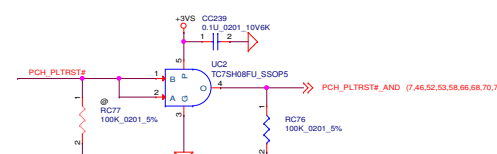
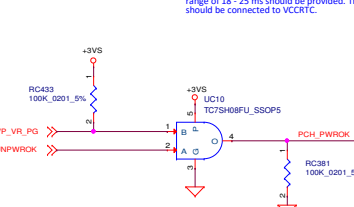
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Issued Date	2015/12/16	Deciphered Date	2016/12/13
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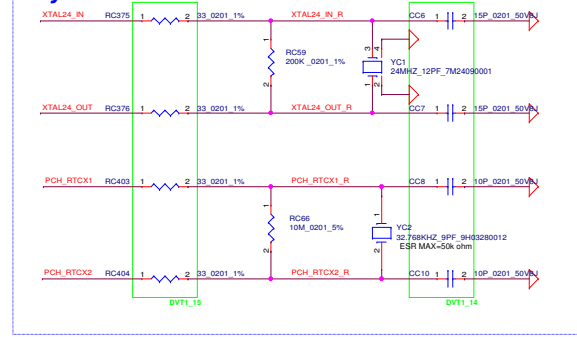
PCH GLITCH ISSUE MITIGATION(PDG p.130)



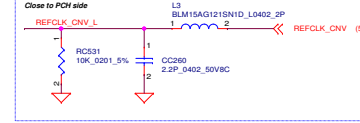
PDG_An RC delay circuit with a time delay in the range of 18 - 25 ns should be provided. The circuit should be connected to VCCRT.



Crystal 24MHz / 32.768KHz



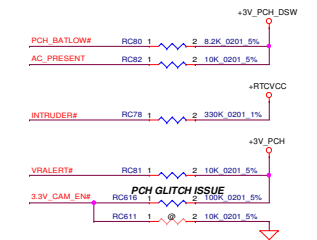
Intel Recommend



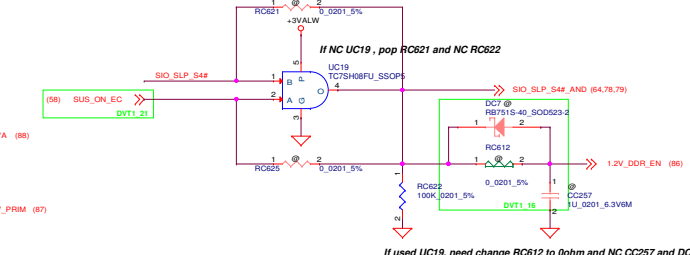
Recommended components:

- Ferrite bead: BLM3AG1215N1 (0201) or BLM3AG1215N1 (0402)
 - Capacitor: High frequency ceramic cap 0402 50V 1.0µF-4.7µF
- The following capacitor values are recommended
- It is recommended to choose the value according to the clock trace length to account for the clock trace capacitance

Clock route length + L	Recommended capacitor values
L < 8"	47pF
8" < L < 9"	2.2pF to 3.3pF
9" < L < 10"	1.0pF to 2.2pF



need check VALERT#

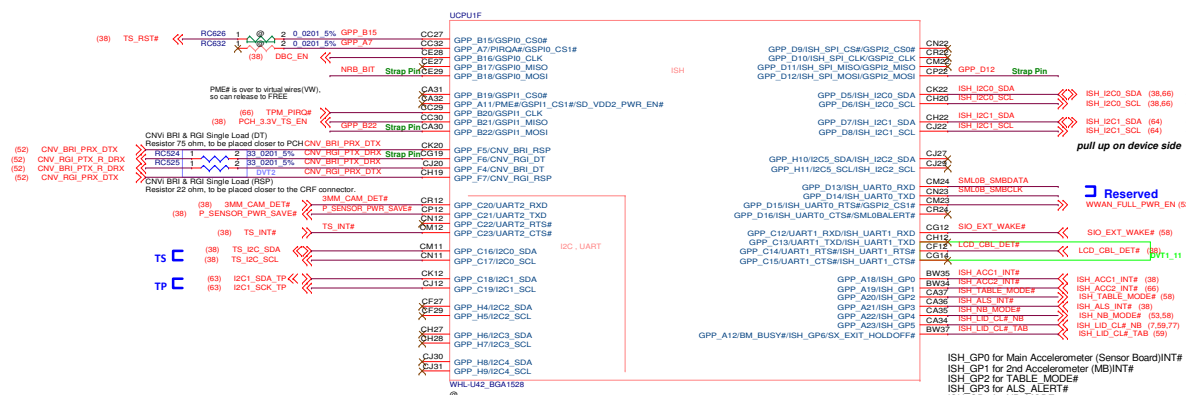
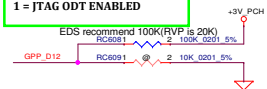


JTAG ODT DISABLE

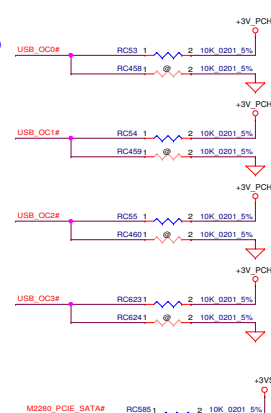
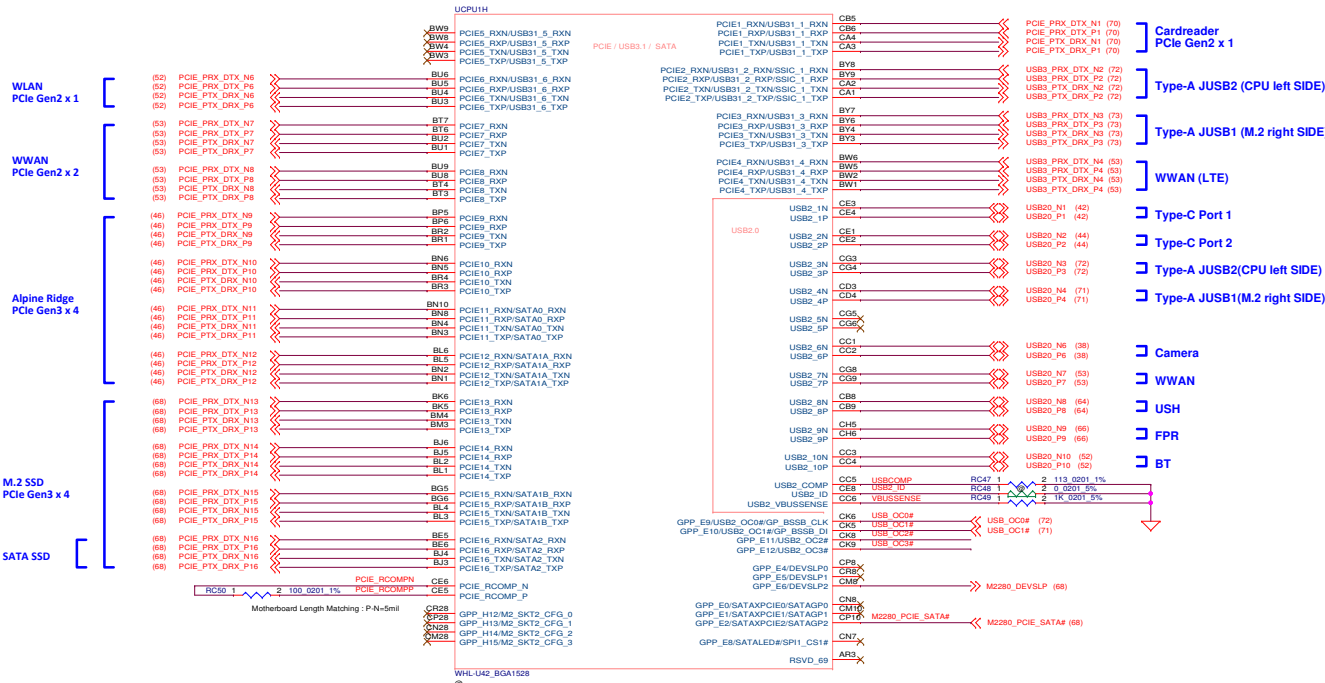
GPP_D12 (WEAK INTERNAL PU)

0 = ITAGE ODT DISABLED

1 = JTAG ODT ENABLED



ISH_GP0 for Main Accelerometer (Sensor Board)INT#
ISH_GP1 for 2nd Accelerometer (MB)INT#
ISH_GP2 for TABLE_MODE#
ISH_GP3 for ALS_ALERT#
ISH_GP4 for NB_MODE#
ISH_GP5 for NB_LID#
ISH_GP6 for TAB_LID#
ISH_GP7 for Proximity sensor(Camera)INT#

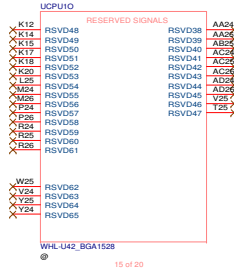


Pin Number	CTL Data	WHL U42 Q6/Production	ICN U42/WHL U42 ESD1
AV28	21W	RSVD	RSVD
T25	VCCOPD_SENSE	RSVD	RSVD
V25	VCCOPD_SENSE	RSVD	RSVD
AA34	VCCOPD	RSVD	RSVD
AA36	VCCOPD	RSVD	RSVD
AA38	VCCOPD	RSVD	RSVD
AA39	VCCOPD	RSVD	RSVD
AA40	VCCOPD	RSVD	RSVD
AA41	VCCOPD	RSVD	RSVD
AA42	VCCOPD	RSVD	RSVD
AA43	VCCOPD	RSVD	RSVD
AA44	VCCOPD	RSVD	RSVD
AA45	VCCOPD	RSVD	RSVD
AA46	VCCOPD	RSVD	RSVD
AA47	VCCOPD	RSVD	RSVD
AA48	VCCOPD	RSVD	RSVD
AA49	VCCOPD	RSVD	RSVD
AA50	VCCOPD	RSVD	RSVD
AA51	VCCOPD	RSVD	RSVD
AA52	VCCOPD	RSVD	RSVD
AA53	VCCOPD	RSVD	RSVD
AA54	VCCOPD	RSVD	RSVD
AA55	VCCOPD	RSVD	RSVD
AA56	VCCOPD	RSVD	RSVD
AA57	VCCOPD	RSVD	RSVD
AA58	VCCOPD	RSVD	RSVD
AA59	VCCOPD	RSVD	RSVD
AA60	VCCOPD	RSVD	RSVD
AA61	VCCOPD	RSVD	RSVD
AA62	VCCOPD	RSVD	RSVD
AA63	VCCOPD	RSVD	RSVD
AA64	VCCOPD	RSVD	RSVD
AA65	VCCOPD	RSVD	RSVD
AA66	VCCOPD	RSVD	RSVD
AA67	VCCOPD	RSVD	RSVD
AA68	VCCOPD	RSVD	RSVD
AA69	VCCOPD	RSVD	RSVD
AA70	VCCOPD	RSVD	RSVD
AA71	VCCOPD	RSVD	RSVD
AA72	VCCOPD	RSVD	RSVD
AA73	VCCOPD	RSVD	RSVD
AA74	VCCOPD	RSVD	RSVD
AA75	VCCOPD	RSVD	RSVD
AA76	VCCOPD	RSVD	RSVD
AA77	VCCOPD	RSVD	RSVD
AA78	VCCOPD	RSVD	RSVD
AA79	VCCOPD	RSVD	RSVD
AA80	VCCOPD	RSVD	RSVD
AA81	VCCOPD	RSVD	RSVD
AA82	VCCOPD	RSVD	RSVD
AA83	VCCOPD	RSVD	RSVD
AA84	VCCOPD	RSVD	RSVD
AA85	VCCOPD	RSVD	RSVD
AA86	VCCOPD	RSVD	RSVD
AA87	VCCOPD	RSVD	RSVD
AA88	VCCOPD	RSVD	RSVD
AA89	VCCOPD	RSVD	RSVD
AA90	VCCOPD	RSVD	RSVD
AA91	VCCOPD	RSVD	RSVD
AA92	VCCOPD	RSVD	RSVD
AA93	VCCOPD	RSVD	RSVD
AA94	VCCOPD	RSVD	RSVD
AA95	VCCOPD	RSVD	RSVD
AA96	VCCOPD	RSVD	RSVD
AA97	VCCOPD	RSVD	RSVD
AA98	VCCOPD	RSVD	RSVD
AA99	VCCOPD	RSVD	RSVD
AA100	VCCOPD	RSVD	RSVD

PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

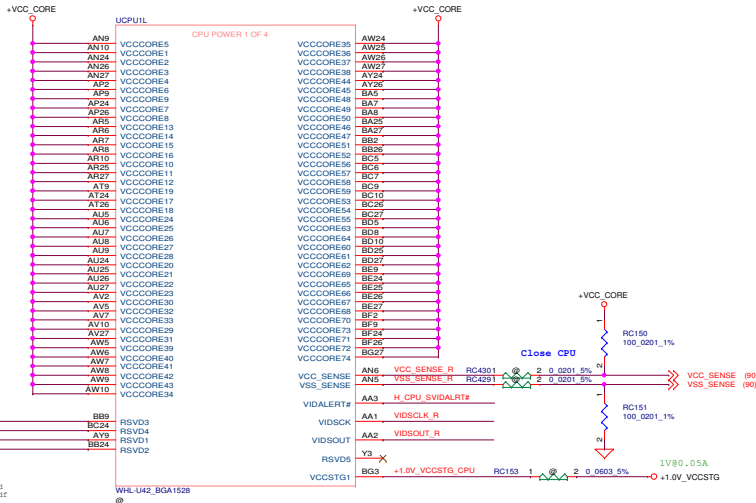
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

+VCC_CORE: 0.55~1.5V, 29A
+VCC_EDRAM: 1V, 2.5A
+V1.8S_EDRAM: 1.8V, 50mA - REMOVE
+VCC_EOPIO: 0.8~1V, 2A - REMOVE

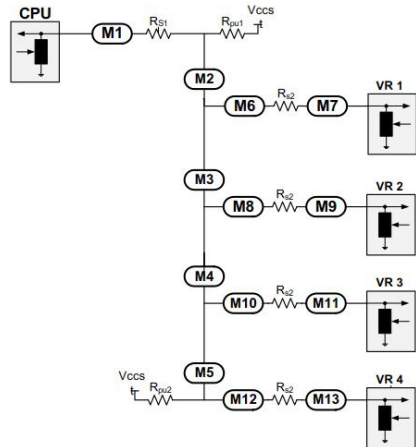


T29 @ PAD-D +1 +VCC_CORE_G0
T30 @ PAD-D +1 +VCC_CORE_G1
T134 @ PAD-D +1 +VCC_CORE_G2
T135 @ PAD-D +1 +VCC_CORE_G3

Jony_12/25: Refer RVP keep it test pad
570990_CFI_U_D084_XVP_C08_sch_savOpd.pdf

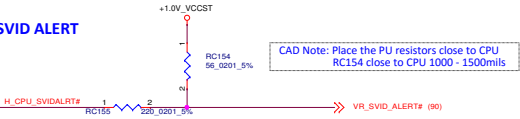


VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)

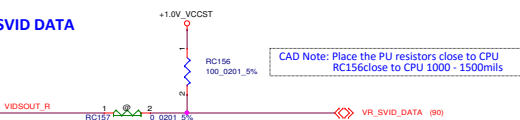


VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω

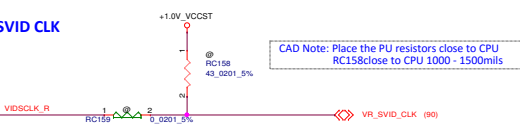
SVID ALERT



SVID DATA



SVID CLK



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Issued Date	Deciphered Date
2015/12/16	2016/12/13

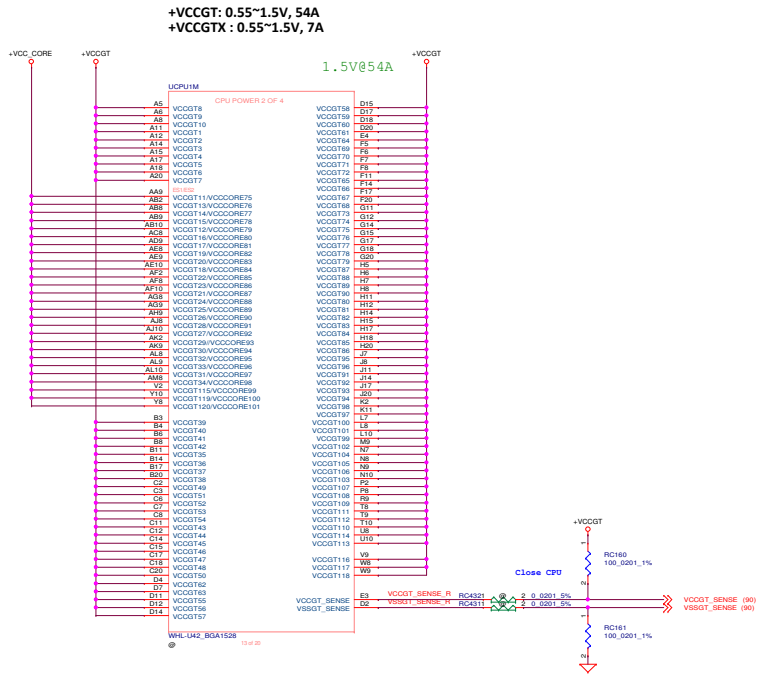
Title
P015 - WHL-U(10/14)CORE Power
Document Number
LA-G441P
Date
Friday, December 14, 2016
Sheet
15 of 100

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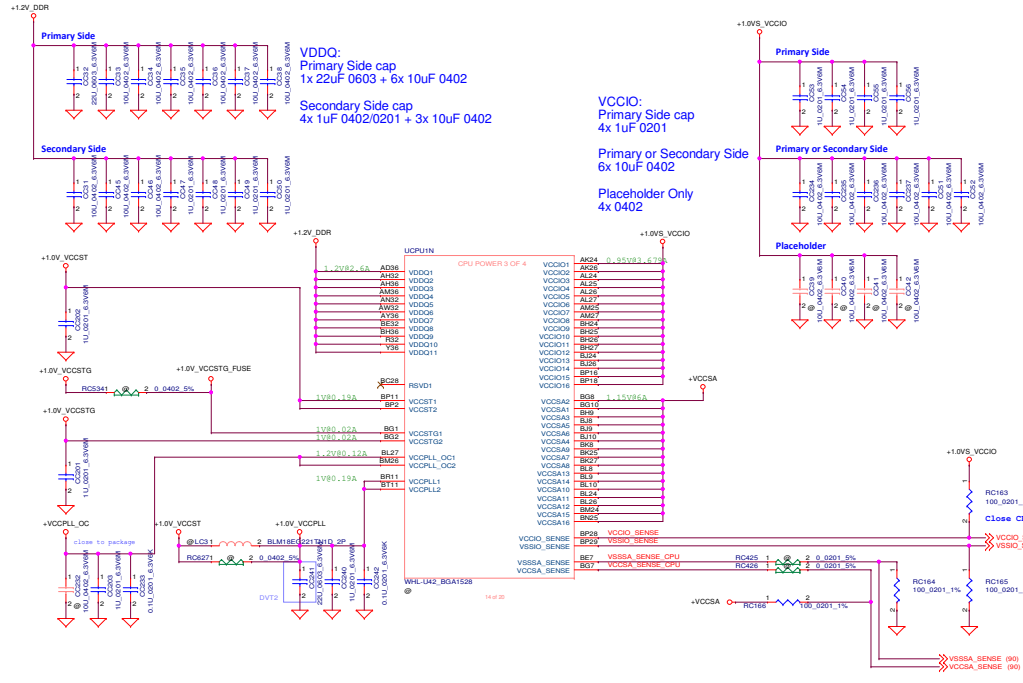
0.1/1000

VCCGT

Pin Number	CPL-U43E	WHL E51 Netname	WHL E52 Netname
AA9	VCCGT	VCCGT	VCCORE
AB10	VCCGT	VCCGT	VCCORE
AB2	VCCGT	VCCGT	VCCORE
AB8	VCCGT	VCCGT	VCCORE
AB9	VCCGT	VCCGT	VCCORE
AC8	VCCGT	VCCGT	VCCORE
AD9	VCCGT	VCCGT	VCCORE
AE10	VCCGT	VCCGT	VCCORE
AE8	VCCGT	VCCGT	VCCORE
AE9	VCCGT	VCCGT	VCCORE
AF10	VCCGT	VCCGT	VCCORE
AF2	VCCGT	VCCGT	VCCORE
AF8	VCCGT	VCCGT	VCCORE
AG8	VCCGT	VCCGT	VCCORE
AG9	VCCGT	VCCGT	VCCORE
AH9	VCCGT	VCCGT	VCCORE
AJ10	VCCGT	VCCGT	VCCORE
AJ8	VCCGT	VCCGT	VCCORE
AK2	VCCGT	VCCGT	VCCORE
AK9	VCCGT	VCCGT	VCCORE
AL10	VCCGT	VCCGT	VCCORE
AL8	VCCGT	VCCGT	VCCORE
AL9	VCCGT	VCCGT	VCCORE
AM8	VCCGT	VCCGT	VCCORE
V2	VCCGT	VCCGT	VCCORE
Y10	VCCGT	VCCGT	VCCORE
Y8	VCCGT	VCCGT	VCCORE

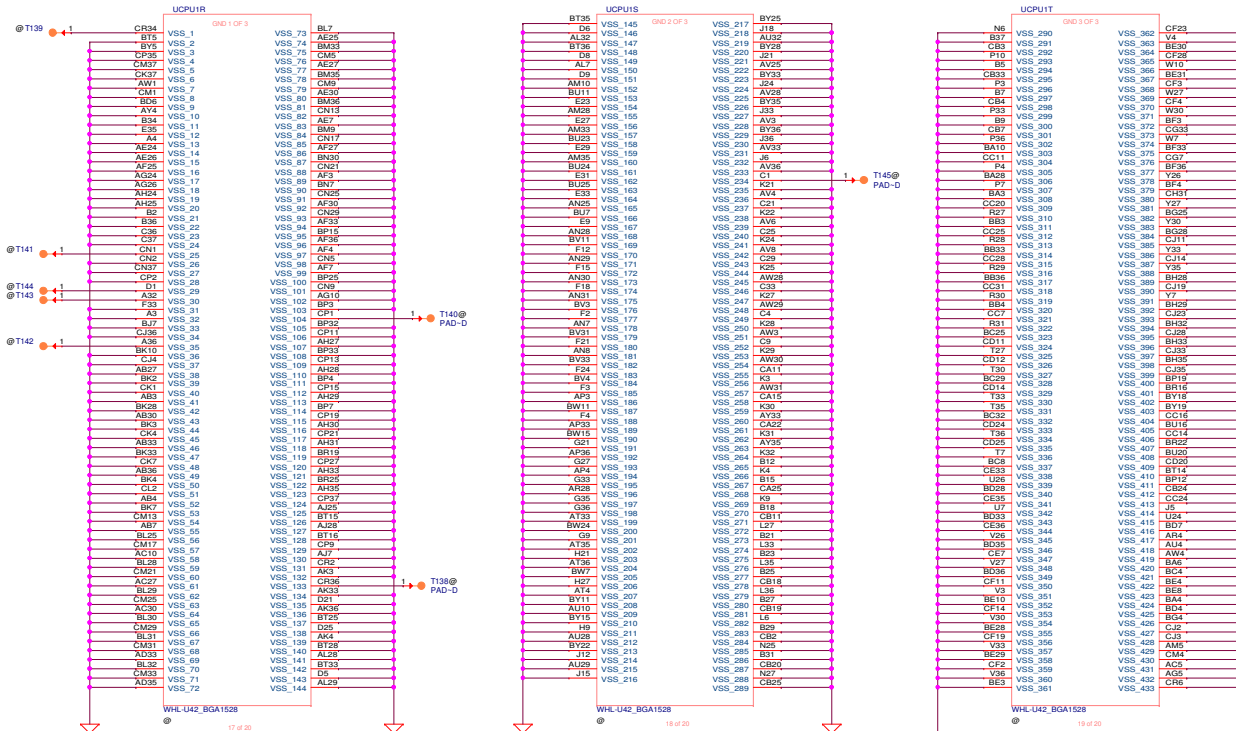


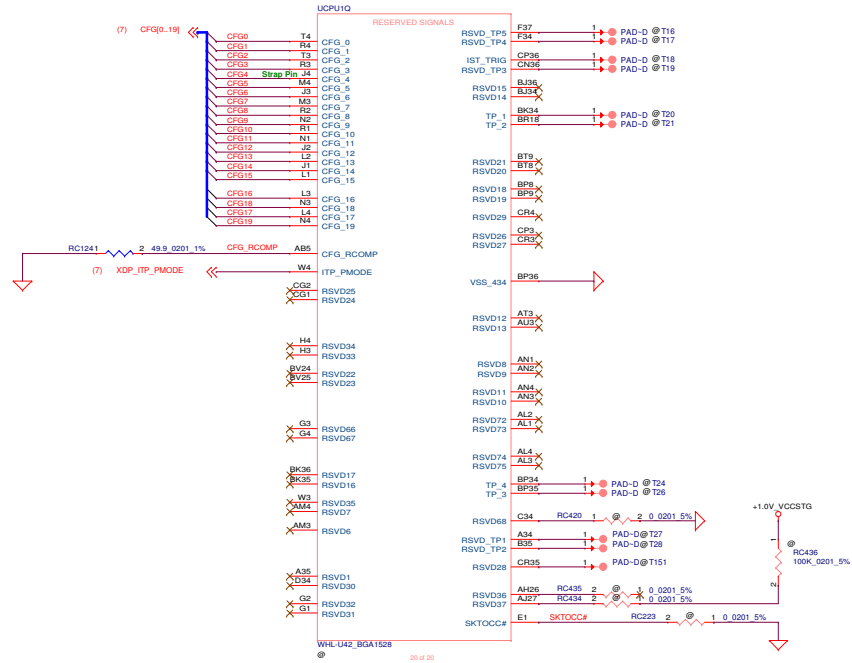
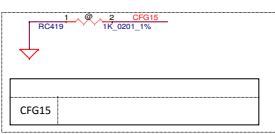
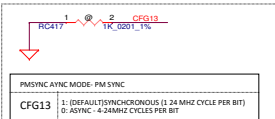
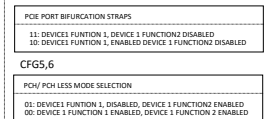
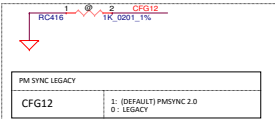
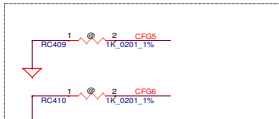
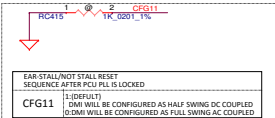
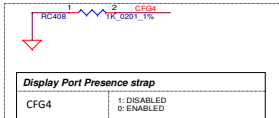
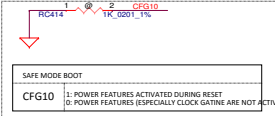
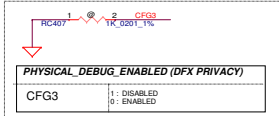
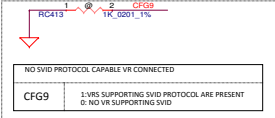
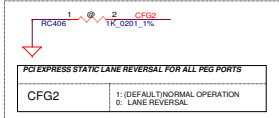
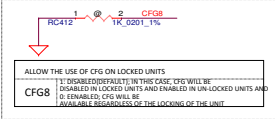
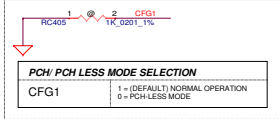
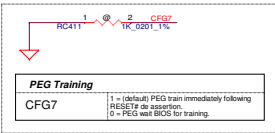
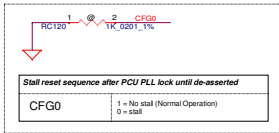
VCCIO / VDDQ



Test pin for Corner NCTF Test(#566757)
need place on CPU corner

Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation







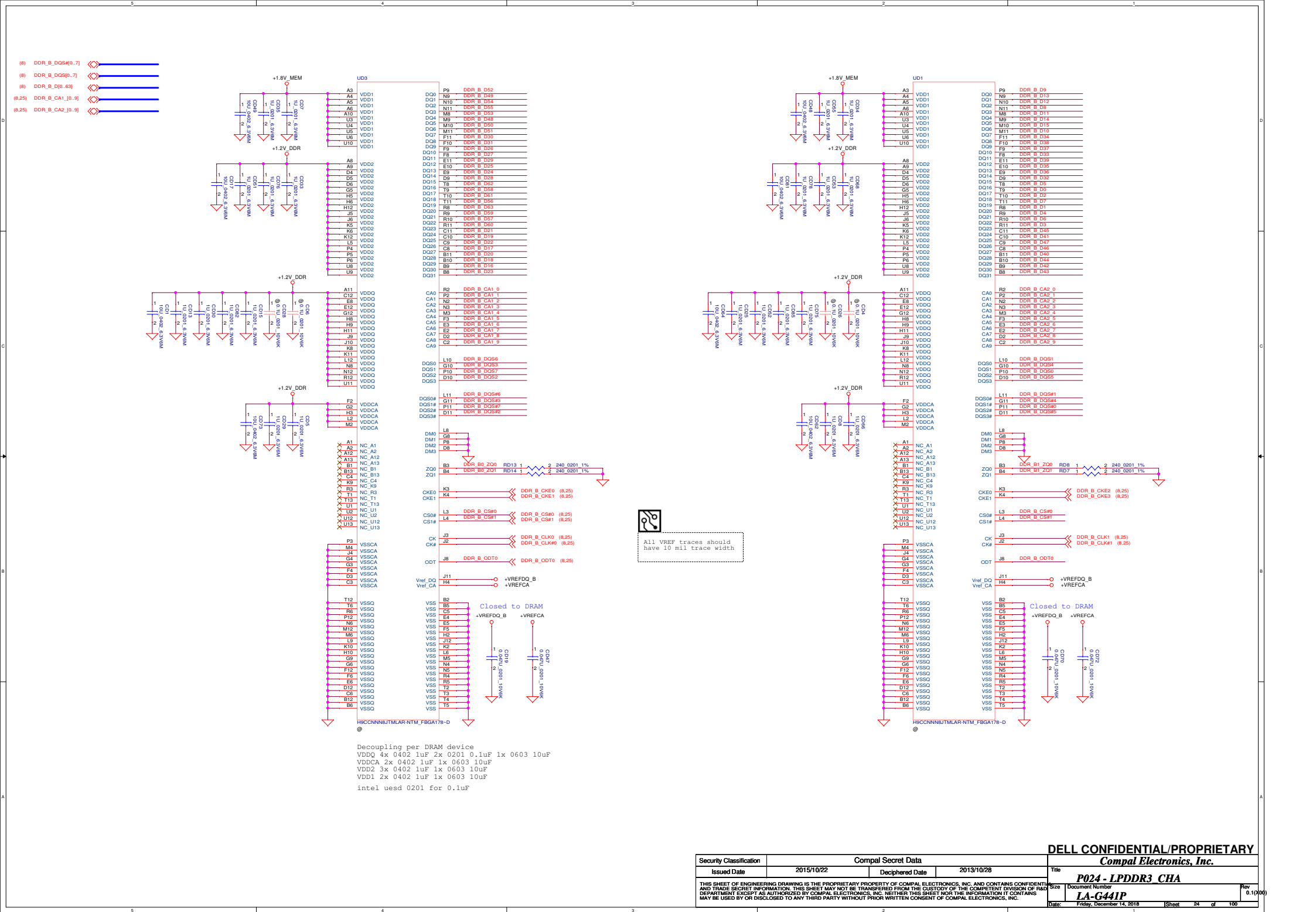
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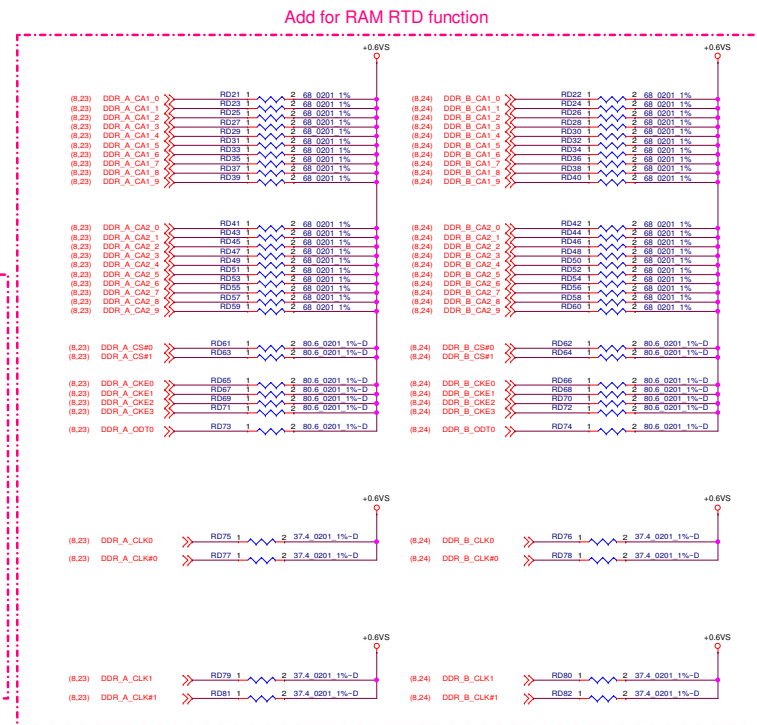
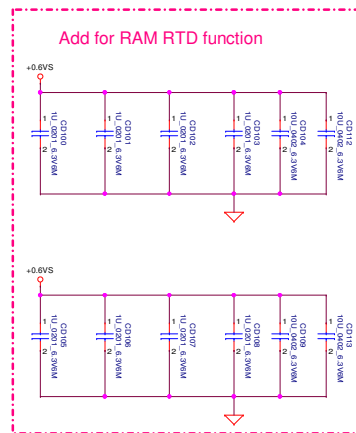
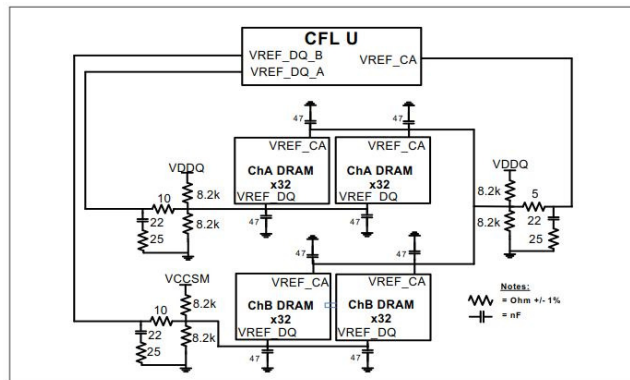
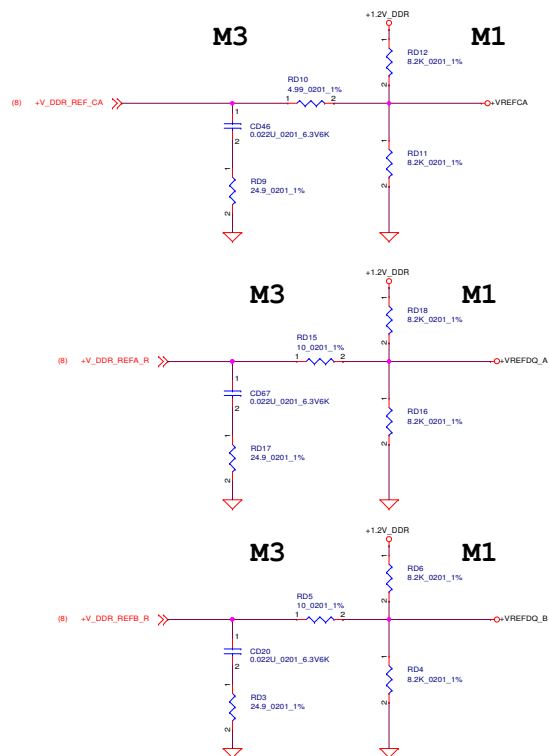
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Title	P024 - LPDDR3 CHA		
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VREF traces should be at least 20 mils wide
with 20 mils spacing to other signals/planes.





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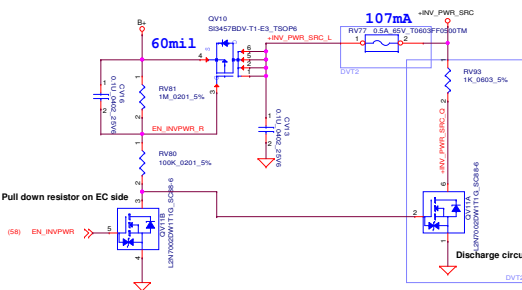


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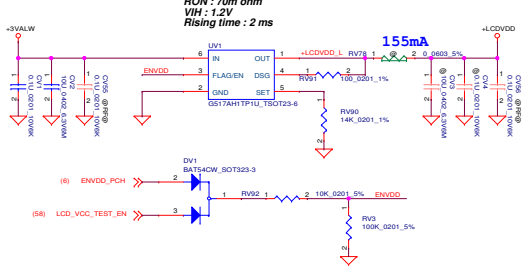


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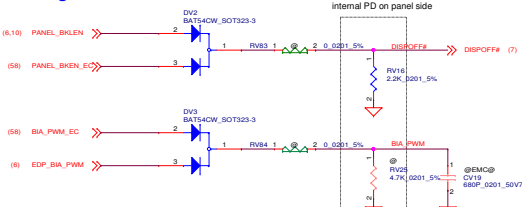
B+ eDP BackLight Power



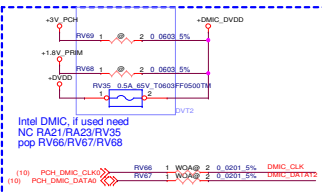
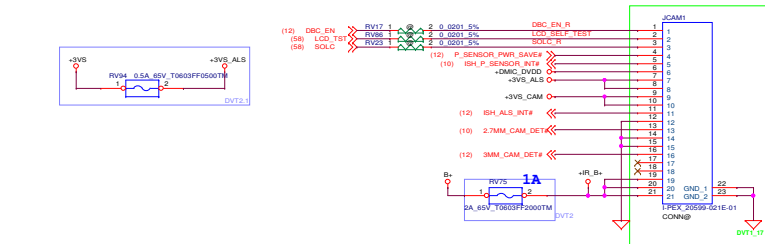
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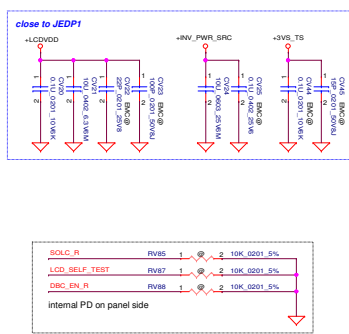
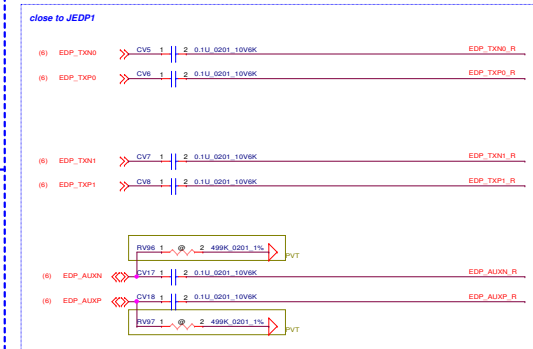
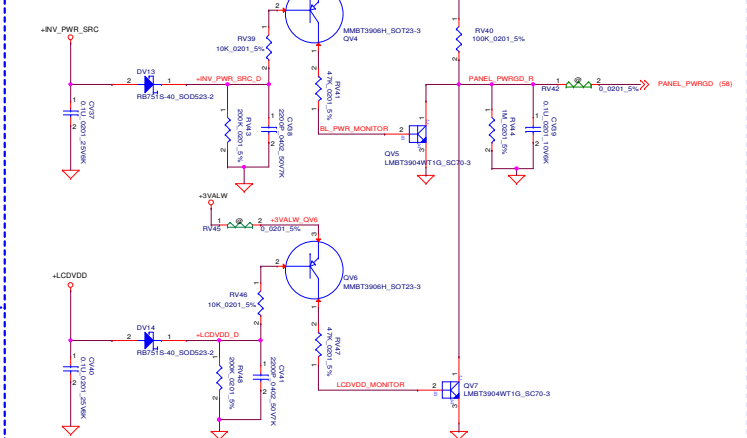
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CAM CONN

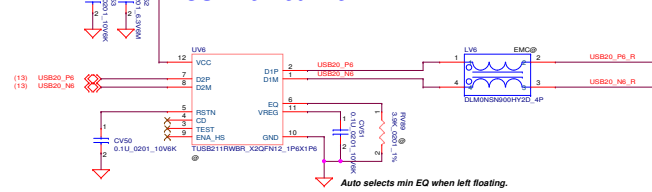


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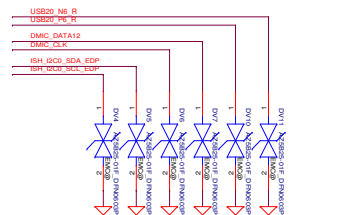


CNT	FN#	Host MEM#	IO	Description	min	max
1	STOP			HIGH: Normal Operation LOW: Stop Scanning Built-in pull-up (to 3.3 volts) resistor 35kOhm	V _{IL} 0.75V _{DD}	V _{OH}
2	IC SDA		IO	IC Data Open drain output: pull-up resistor at Host is needed	V _{IL} 1.35 V _{DD}	V _{OH} 0.25V _{DD}
3	IC SCL		IO	IC Clock Open drain output: pull-up resistor at Host is needed	V _{IL} 1.35 V _{DD}	V _{OH} 0.4
4	NC			No Connection		
5	NC			No Connection		
6	IC IRQ		IO	IC Data Ready Output "LOW" when data ready to send Open drain output: pull-up resistor at Host is needed	V _{IL} 1.35 V _{DD}	V _{OH}
7	RESET		IO	Hardware RESET - Low Active Stop operation when pull "LOW" Built-in pull-up (to 3.3 volts) resistor 10kOhm	V _{IL} 0	0.4
8	VDD +3.3V			3.3 volts (typ) power input	3.14	3.45
9	NC			No Connection		
10	DSND			Drumset		

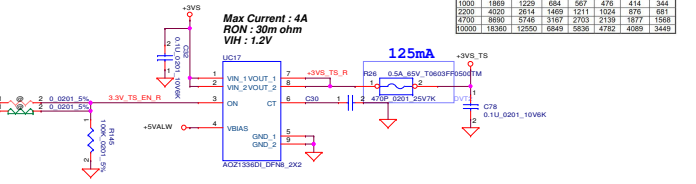
USB2.0 Redriver



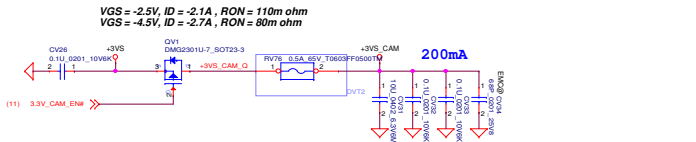
For ESD request



3VS_TS



3VS_CAM

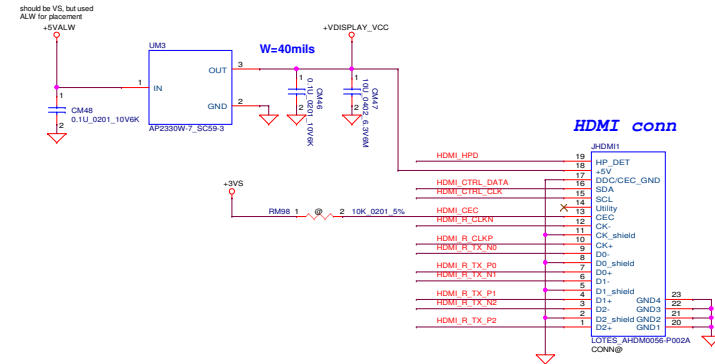
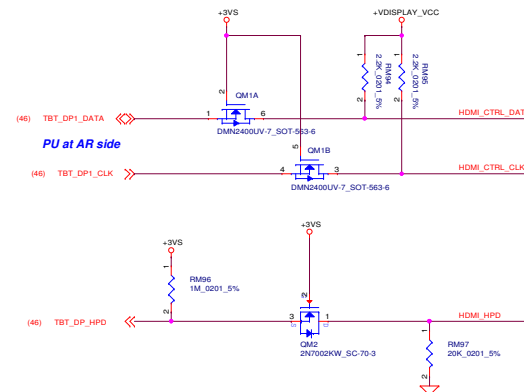
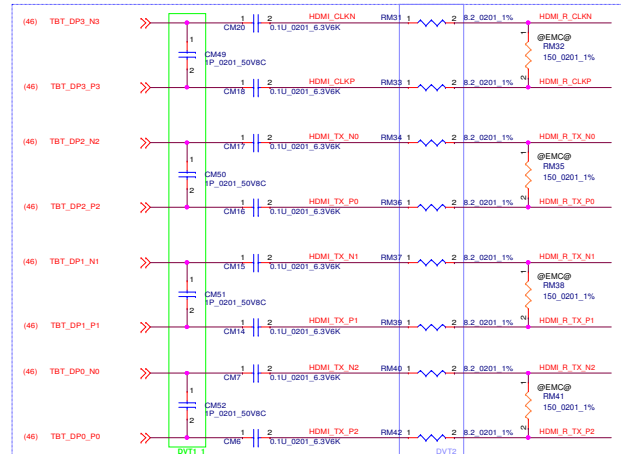


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P038 - eDP/DMIC / Camera			
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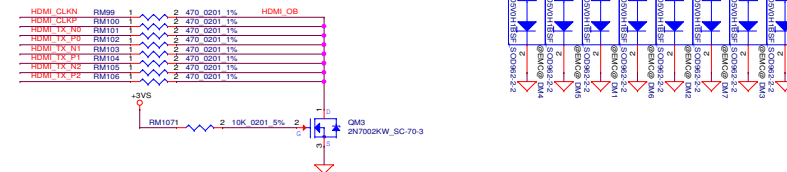


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Place close to JHDMI1



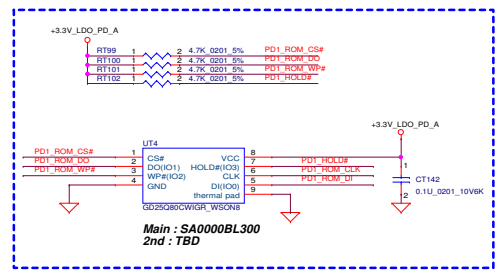
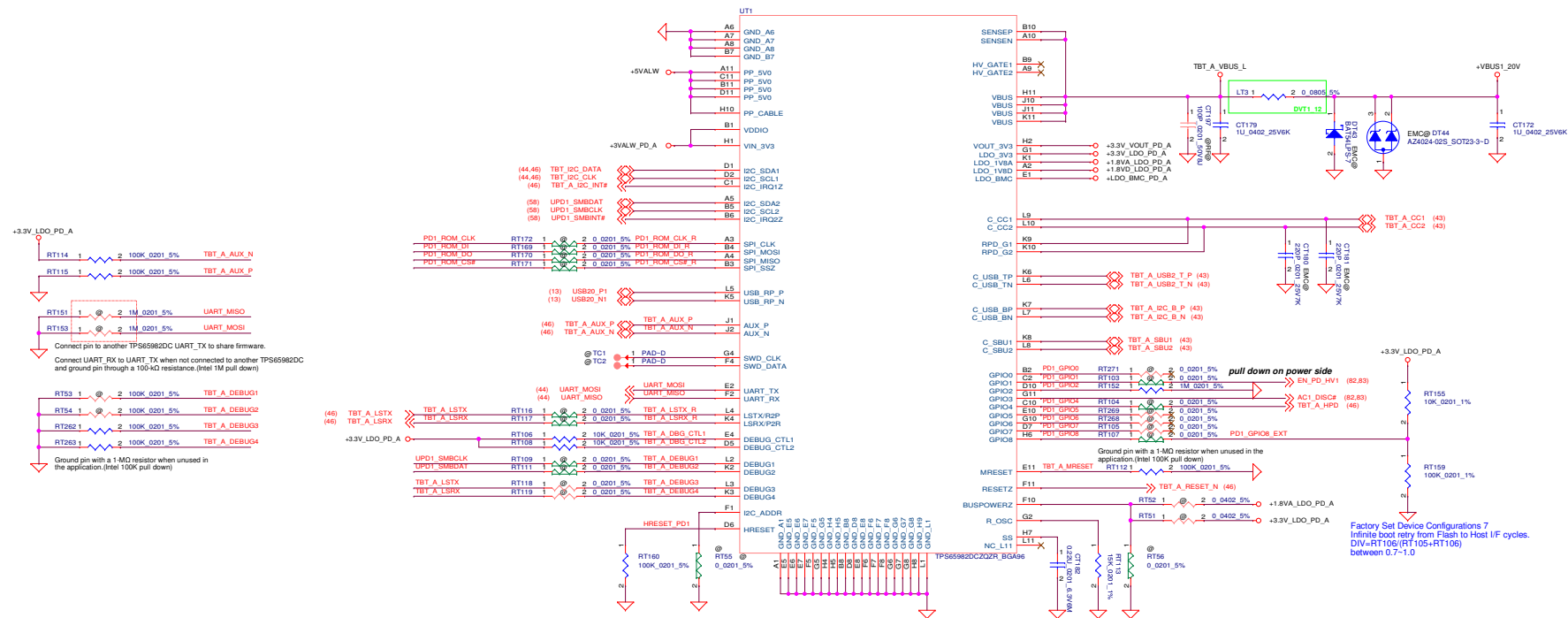
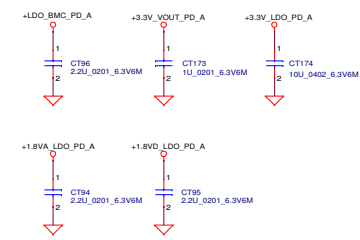
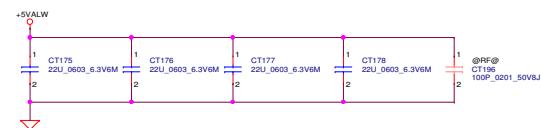
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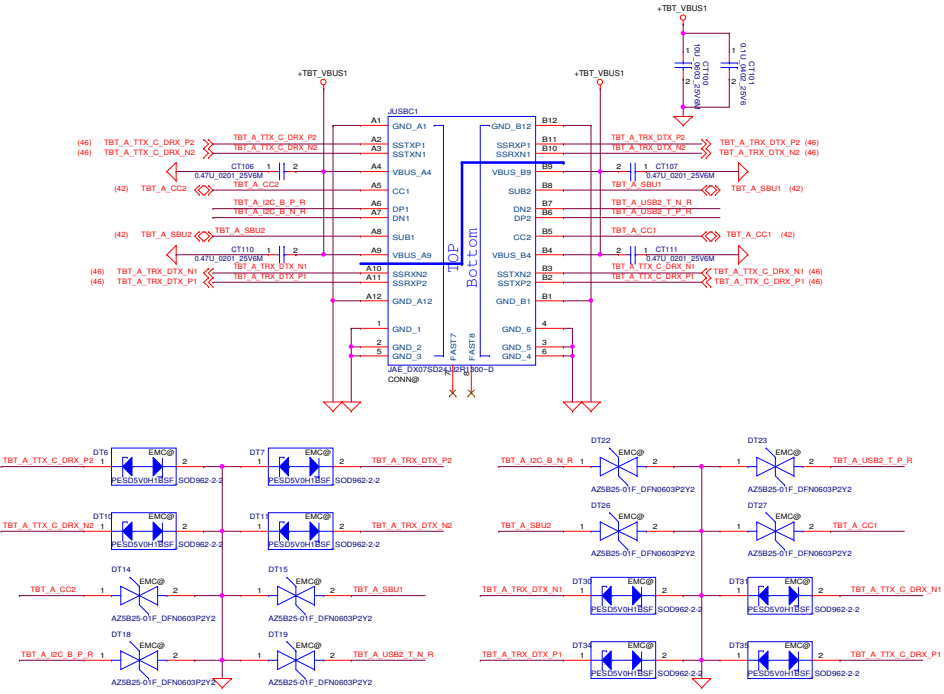
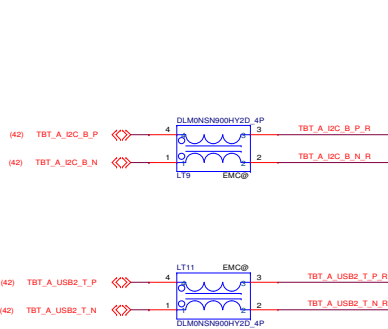
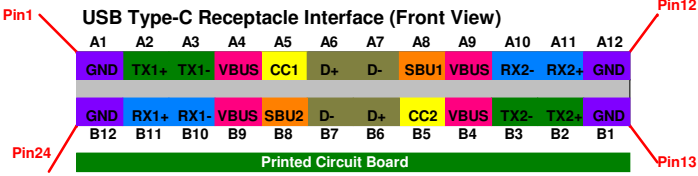


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				Date: Friday, December 14, 2018	
				Sheet 41 of 100	

VIN_3V3 source for dead battery
Placement in bottom side



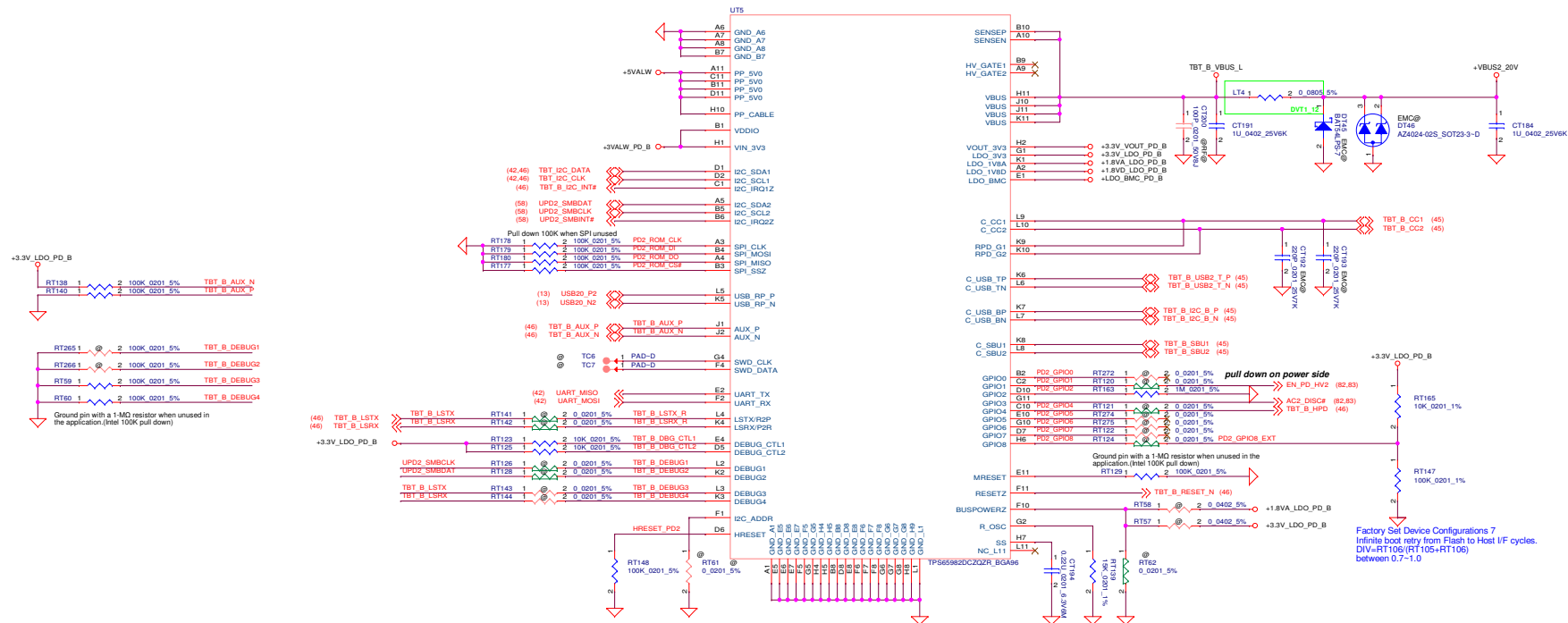
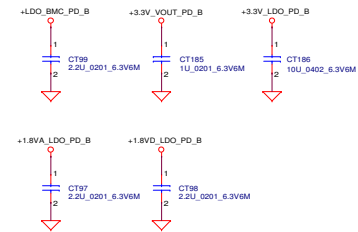
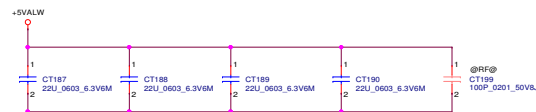
Type-C Port-A



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Title	P043 - TYPE-C PortA_CONN		
Size	Document Number	Rev	0.10000
Date	Friday, December 14, 2016	Sheet	43 of 100

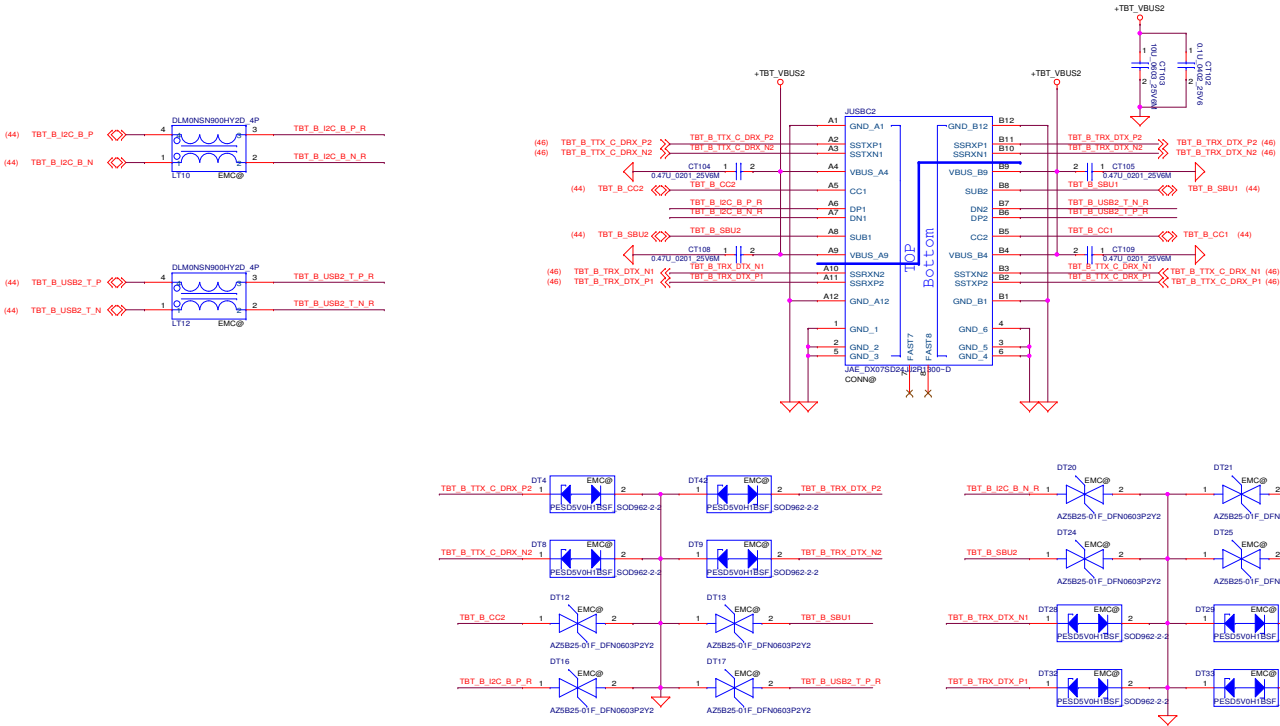
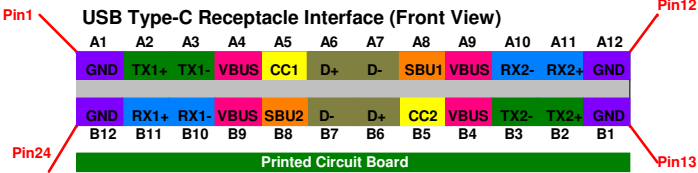
VIN_3V3 source for dead battery
Placement in bottom side



Factory Set Device Configurations 7
Infinite boot retry from Flash to Host I/F cycles
 $DIV=RT106/(RT105+RT106)$
between 0.7-1.0

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Type-C Port-B



Check done on 0416

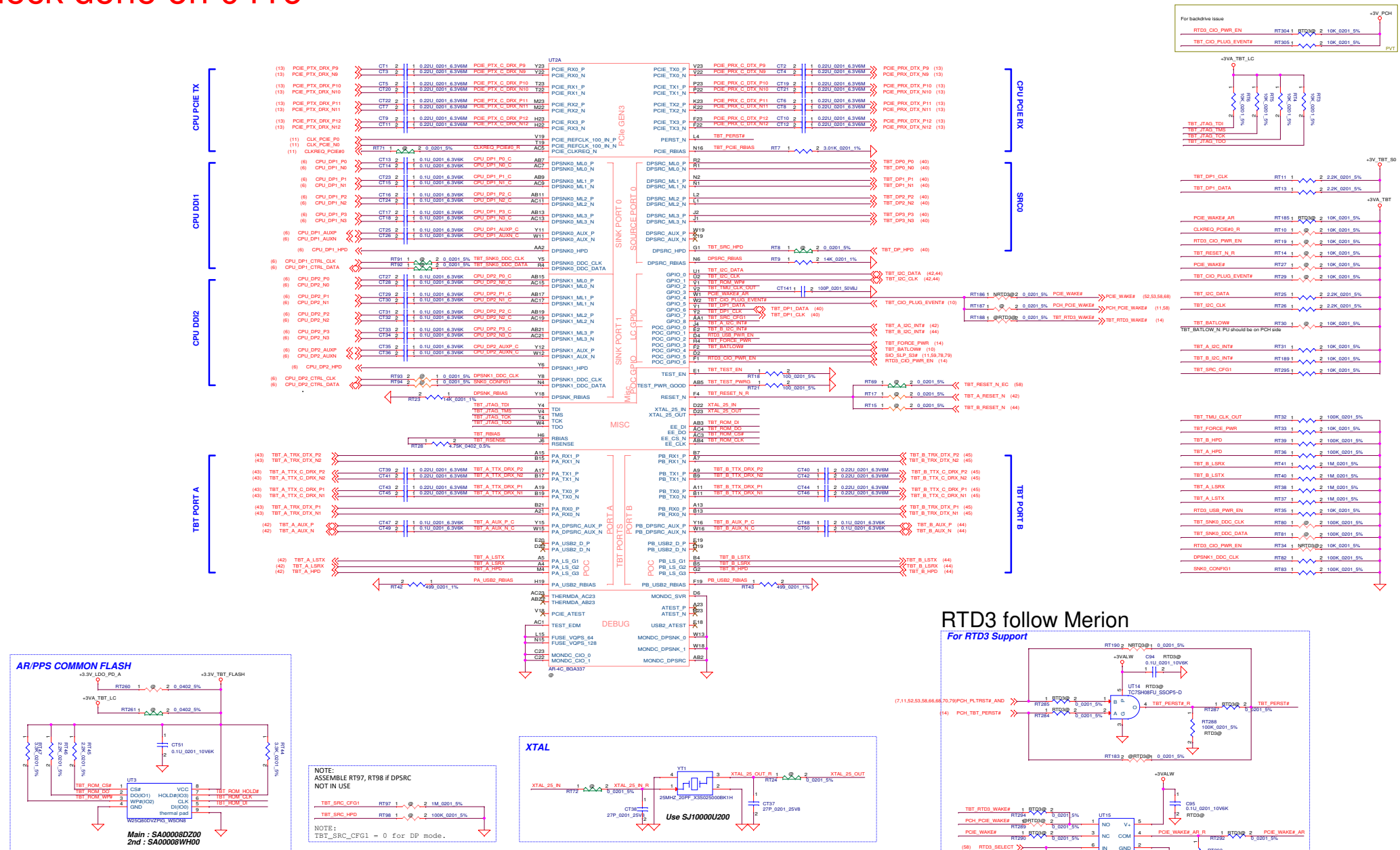
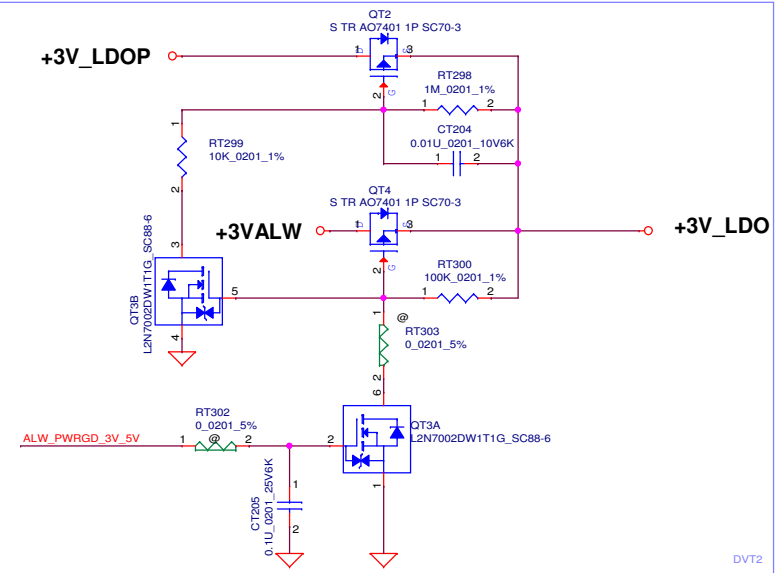
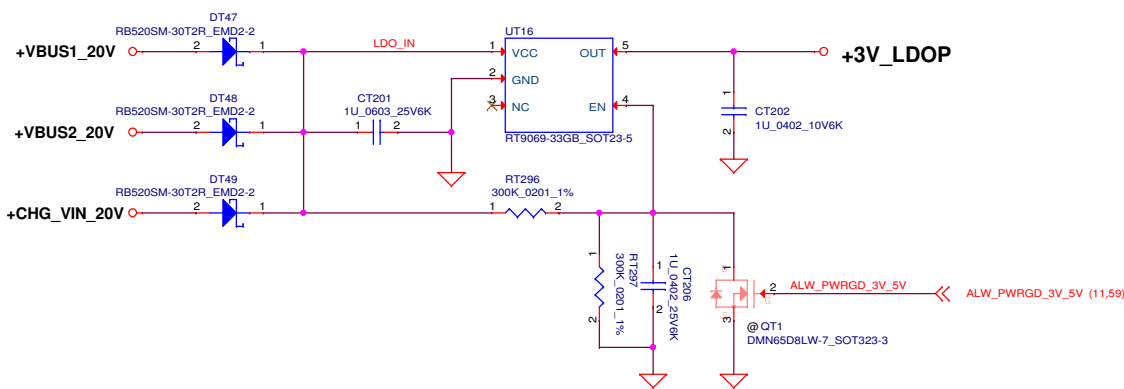


Table 1. Function Table

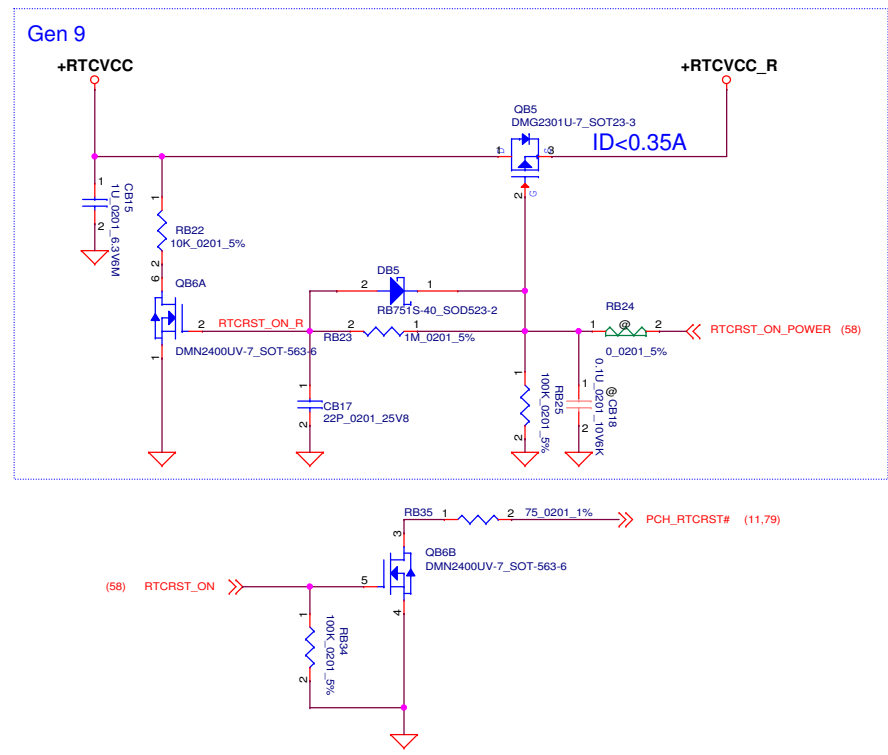
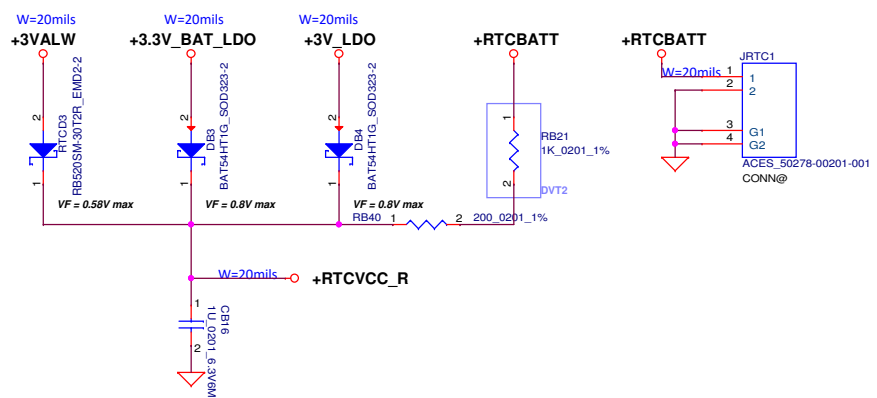
IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

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3V_LDO power



RTC



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		Size	Document Number						Rev	
			LA-G441P						0.1(X00)	
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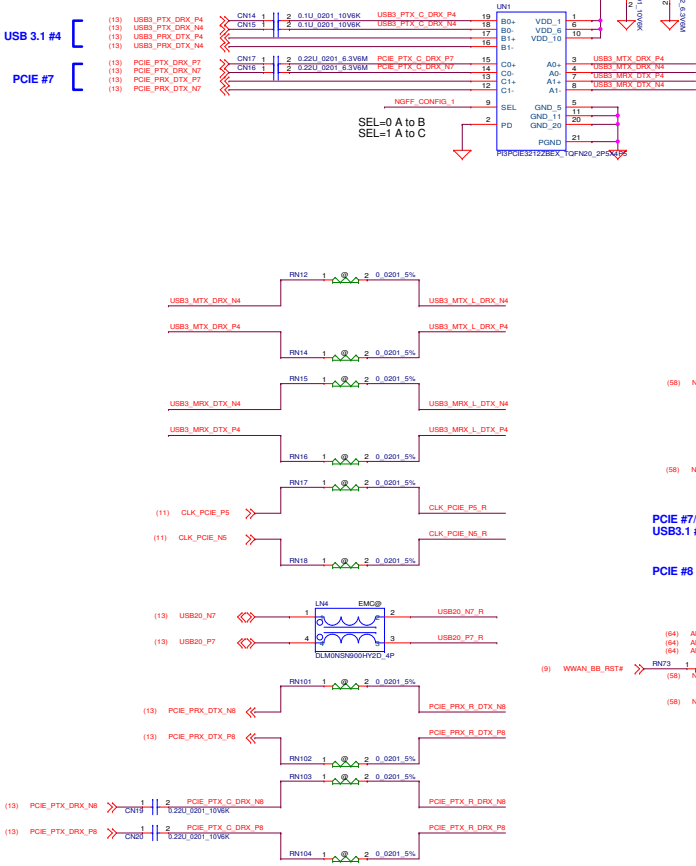
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LA-G441P

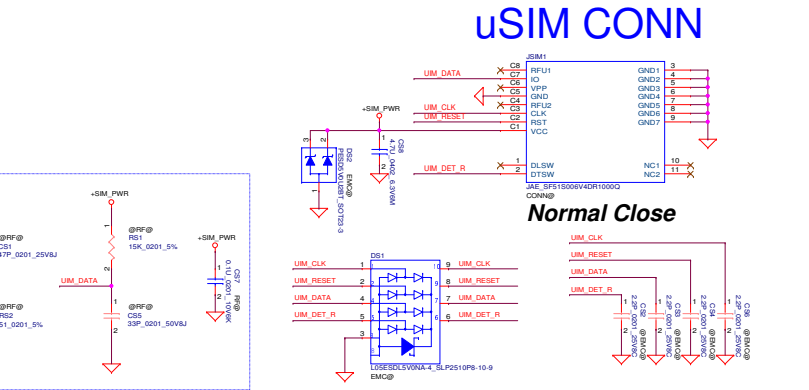
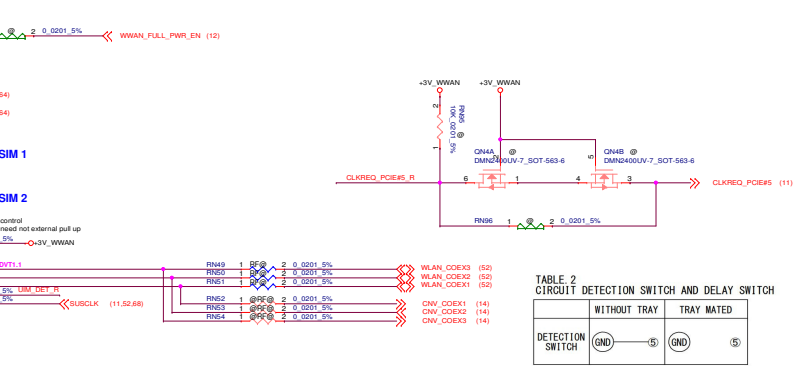
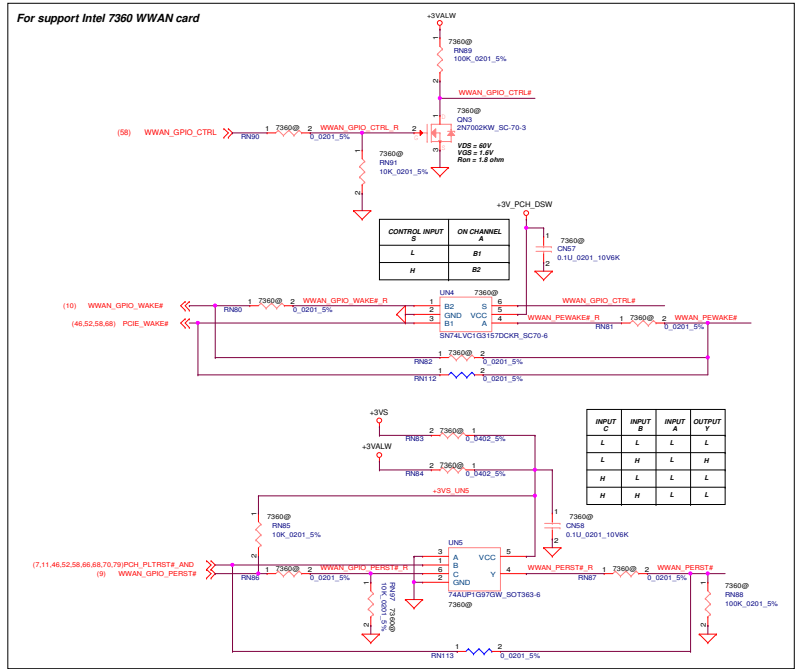
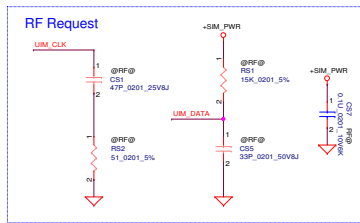
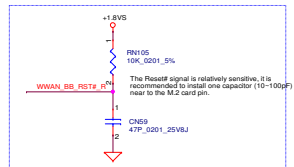
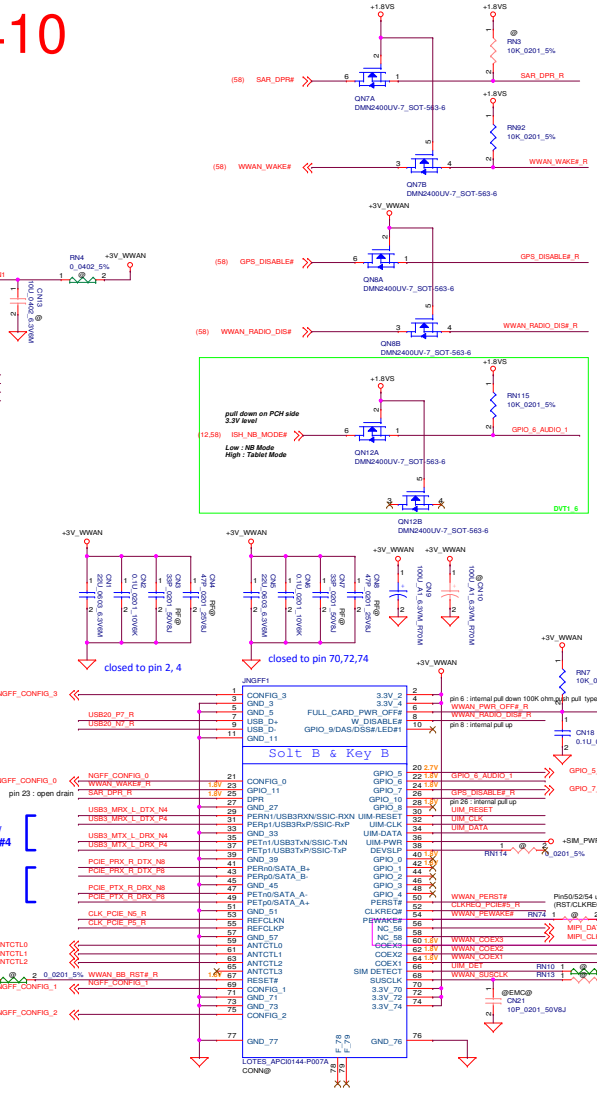
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PCIe/USB 3.0 Mux

USB 3.1 #4
PCIe #7



State#	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	Port Configuration
0	(Pin 21)	(Pin 59)	(Pin 75)	(Pin 1)	SSD - SATA	N/A
1	GND	HIGH	GND	GND	SSD - PCIe	N/A
2	GND	GND	HIGH	GND	WWAN - PCIe	0
3	GND	HIGH	HIGH	GND	WWAN - USB 3.0	0
4	GND	GND	GND	HIGH	WWAN - USB 3.0	1
5	GND	HIGH	GND	HIGH	WWAN - USB 3.0	2
6	GND	GND	HIGH	HIGH	WWAN - USB 3.0	3
7	GND	HIGH	HIGH	HIGH	WWAN - SSIC	0
8	HIGH	GND	GND	GND	WWAN - SSIC	1
9	HIGH	HIGH	GND	GND	WWAN - SSIC	2
10	HIGH	GND	HIGH	GND	WWAN - SSIC	3
11	HIGH	HIGH	HIGH	GND	WWAN - PCIe	0
12	HIGH	GND	GND	HIGH	WWAN - PCIe	1
13	HIGH	HIGH	GND	HIGH	WWAN - PCIe	2
14	HIGH	GND	HIGH	HIGH	DDP/HCA - PCIe	N/A
15	HIGH	HIGH	HIGH	HIGH	No Module	N/A



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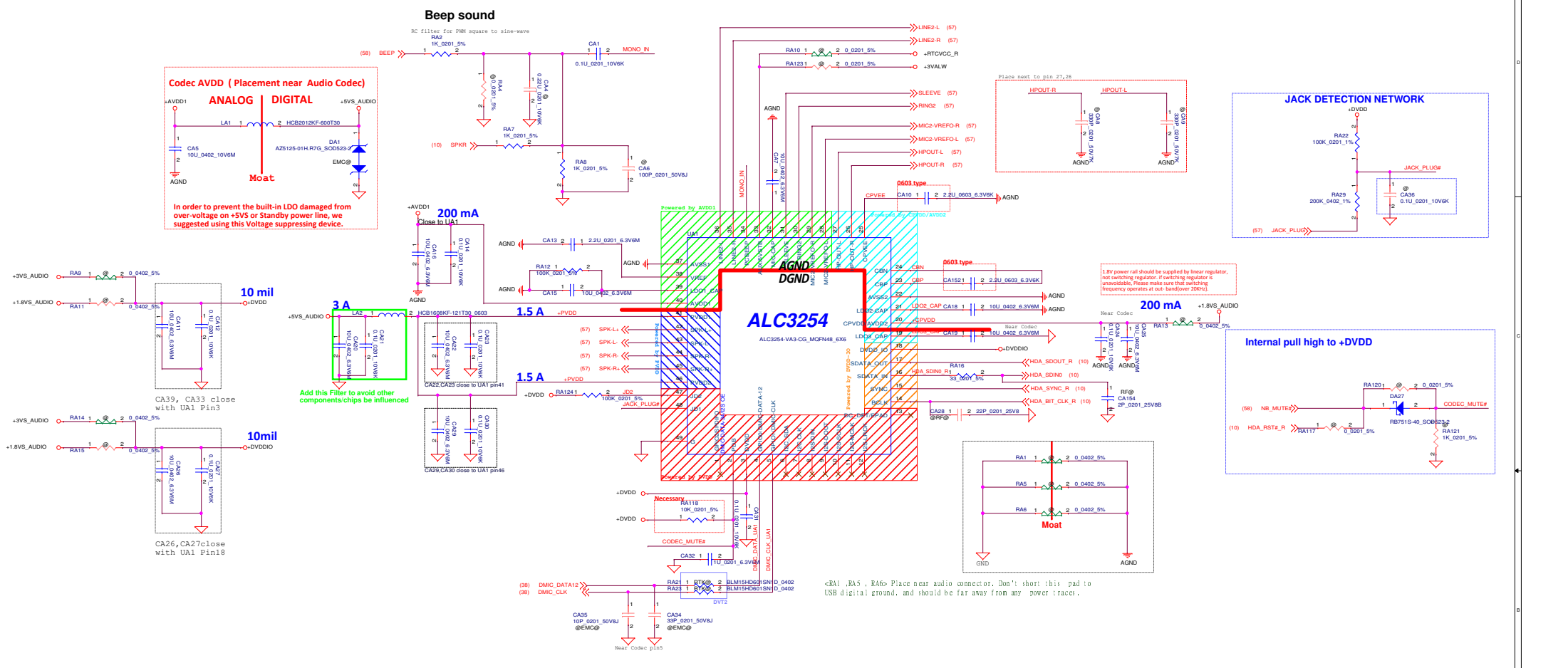


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										54 of 100	

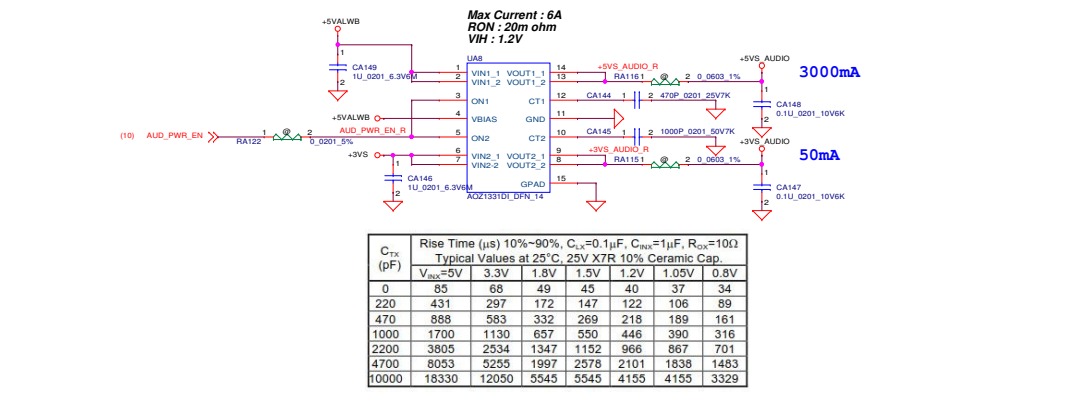


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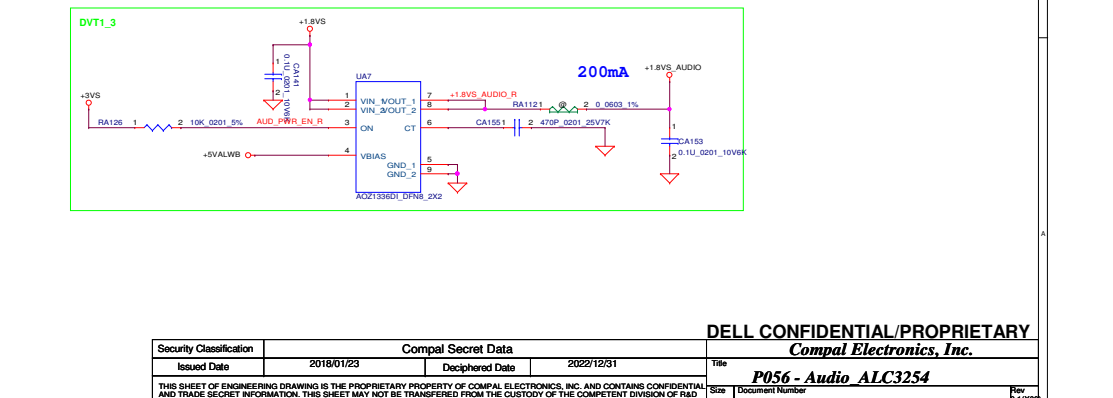
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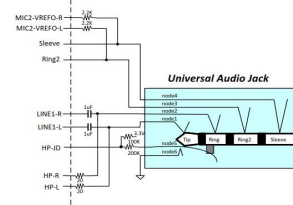
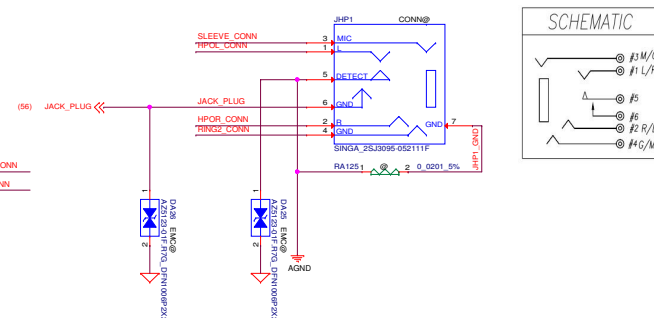
5VS_AUDIO & 3VS_AUDIO



1.8VS_AUDIO



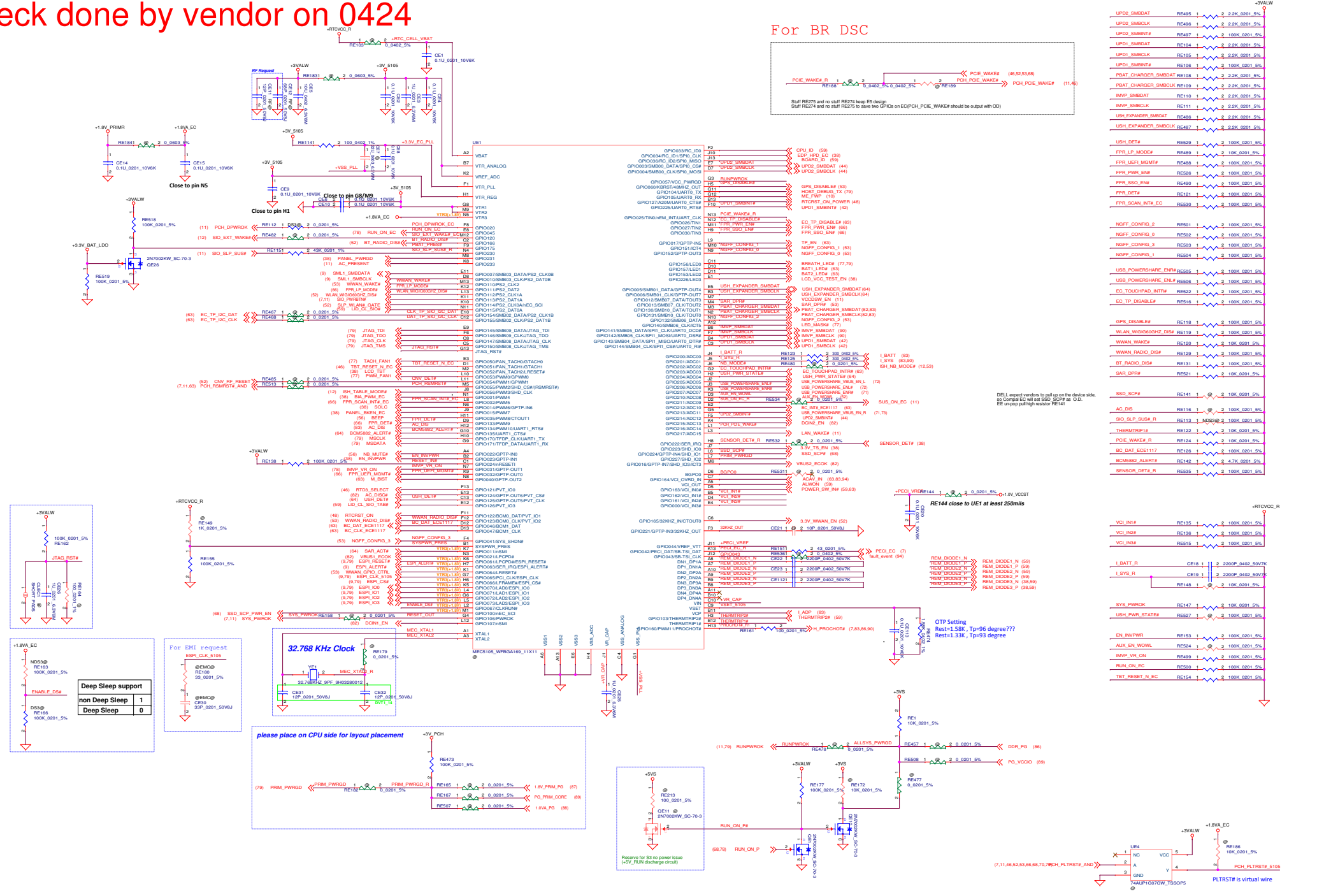
Int. Speaker Conn.

**Universal Audio Jack CONN**

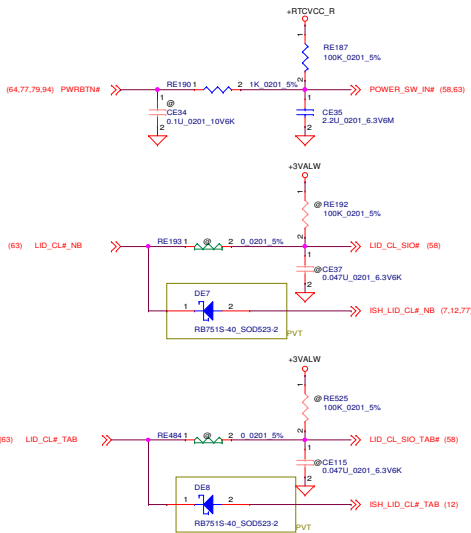
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Issued Date	2018/01/23	Deciphered Date	2022/12/31	Title	<i>P057 - Audio Jack/Speaker</i>
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				<i>EIA-G441P</i>	
				Rev. 001, 2018	Sheet 67 of 190

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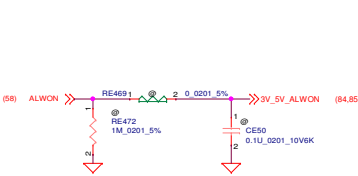
For BR DSC



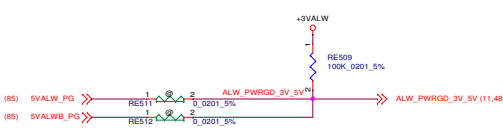
Power SW / NB_LID



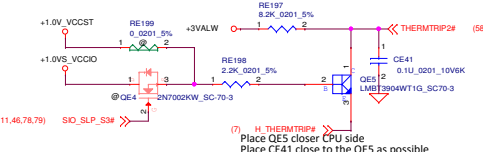
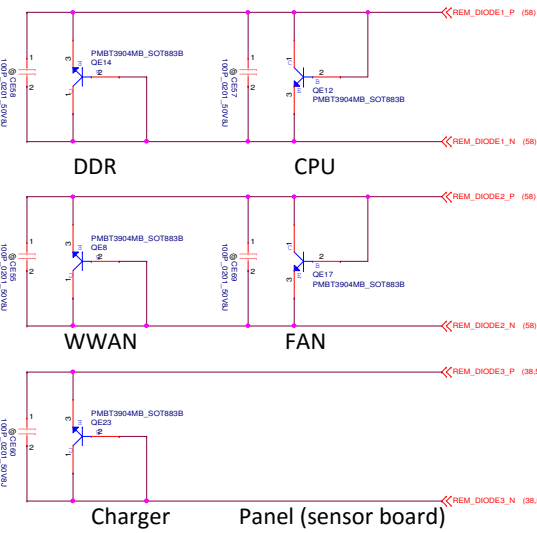
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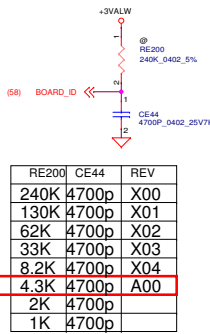
Thermal



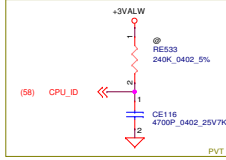
Thermal diode mapping

MEC5105 pins	thermal diode	Location
DP1/DN1	QE12	CPU(OTP,Tp=96)
DN1a/DP1a	QE14	DDR
DP2/DN2	QE17	FAN
DN2a/DP2a	QE8	WWAN
DP3/DN3	QE24	Panel (sensor board)
DN3a/DP3a	QE23	Charger
DP4/DN4	QE22	NC
DN4a/DP4a	QE25	NC

Board ID



RE200	CE44	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
4.3K	4700p	A00
2K	4700p	
1K	4700p	



RE533	CE116	REV
240K	4700p	V-PRO I5
130K	4700p	V-PRO I7
62K	4700p	Non V-PRO I5
33K	4700p	Non V-PRO I7
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

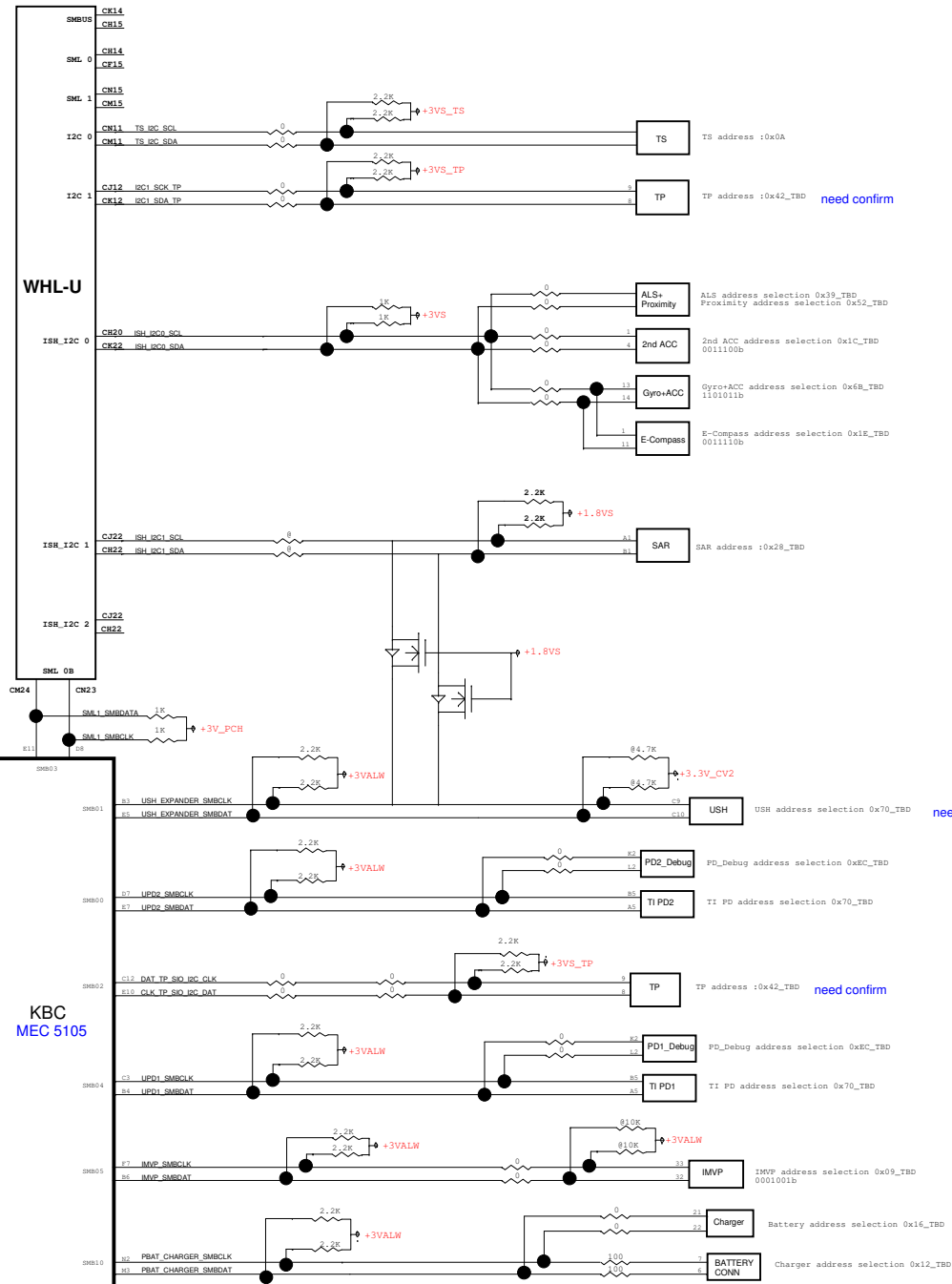
BOARD_ID rise time is measured from 5%~68%.

CPU_ID rise time is measured from 5%~68%.

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WHL-U

KBC
MEC 5105

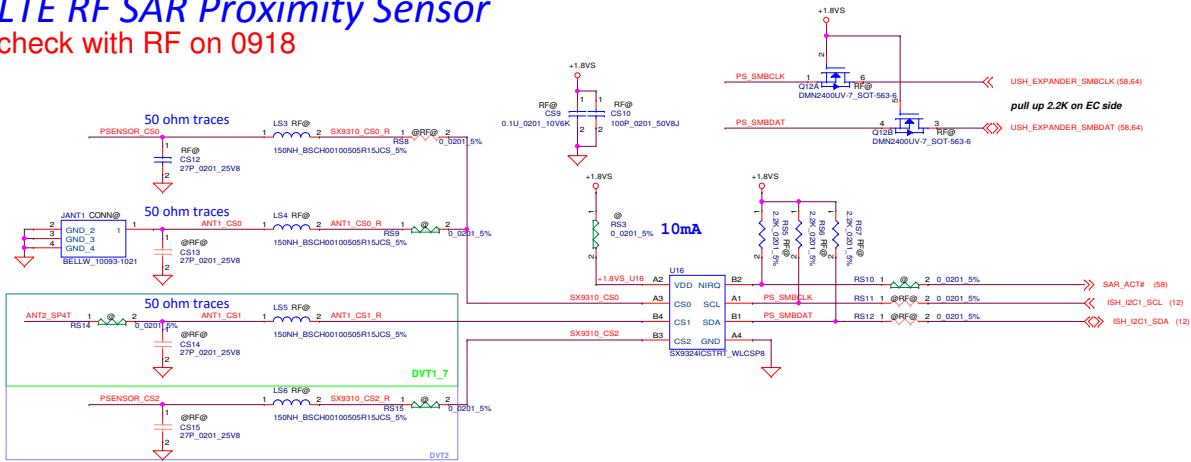


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PART NO. LA-G441P				Rev	110000

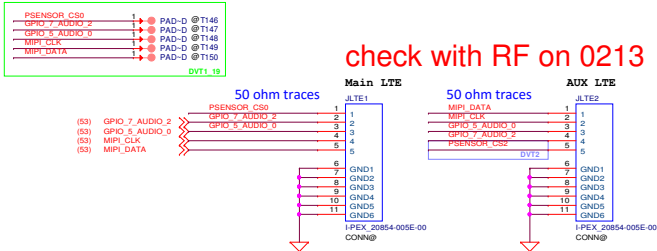


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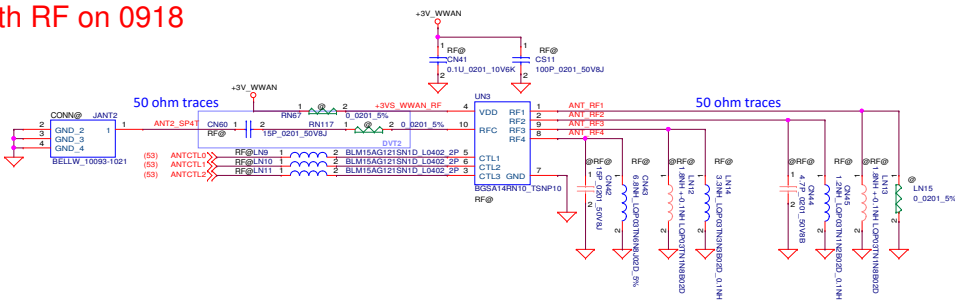
LTE RF SAR Proximity Sensor
check with RF on 0918



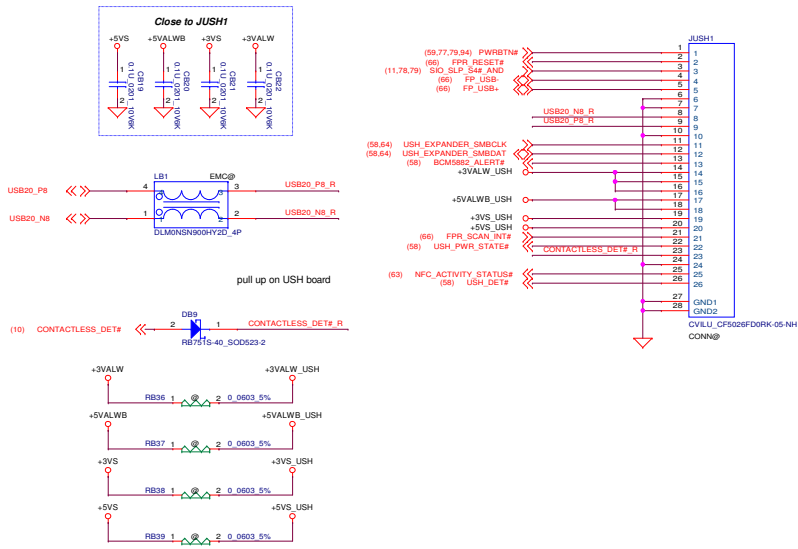
JLTE1/2 CONN



LTE SW SP4T Tunnable IC
check with RF on 0918



USH CONN

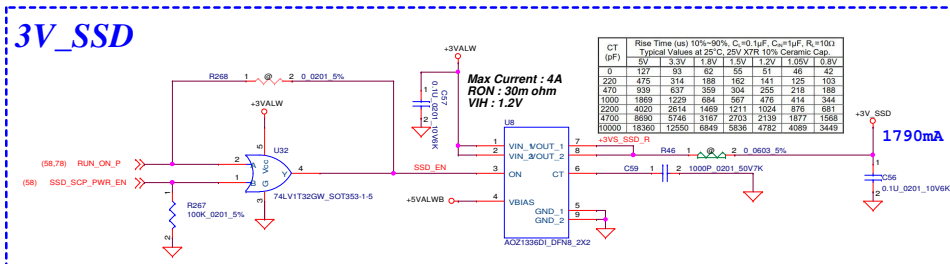
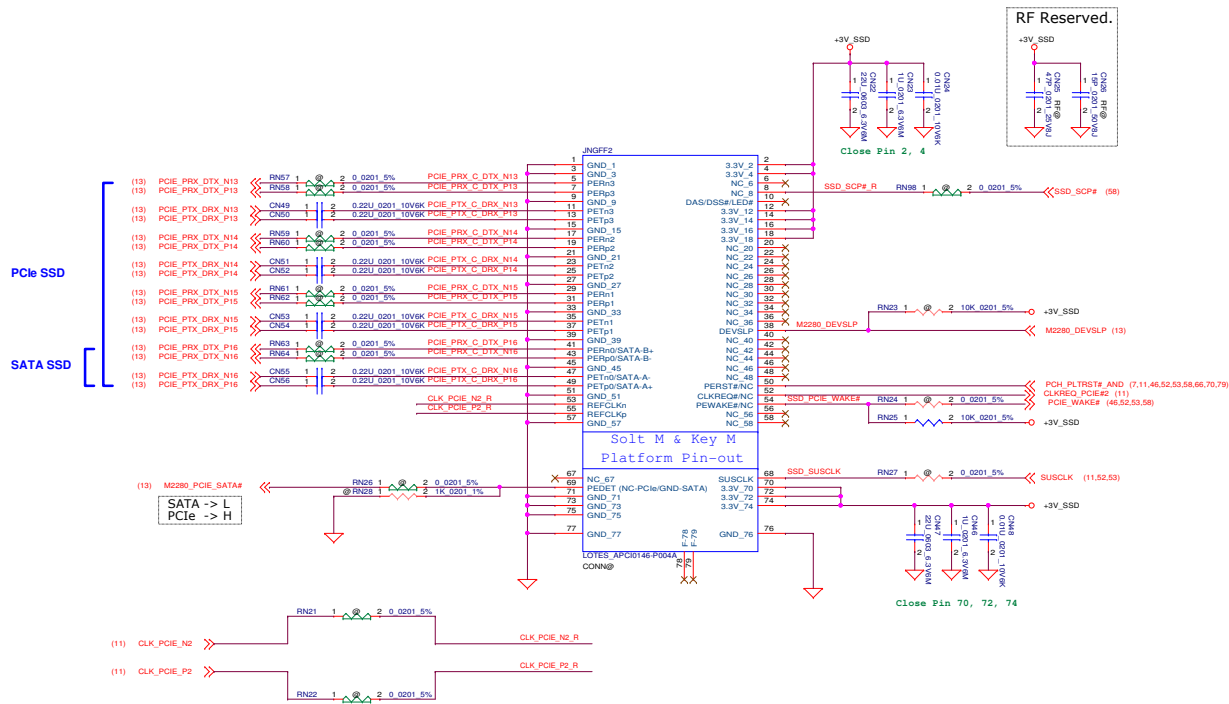




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Date:		Friday, December 14, 2018			0.1(X00)
Sheet		65	of	100	



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						Size		Document Number		Rev	
						LA-G441P		0.1(X00)			
						Date:		Friday, December 14, 2018		Sheet 67 of 100	

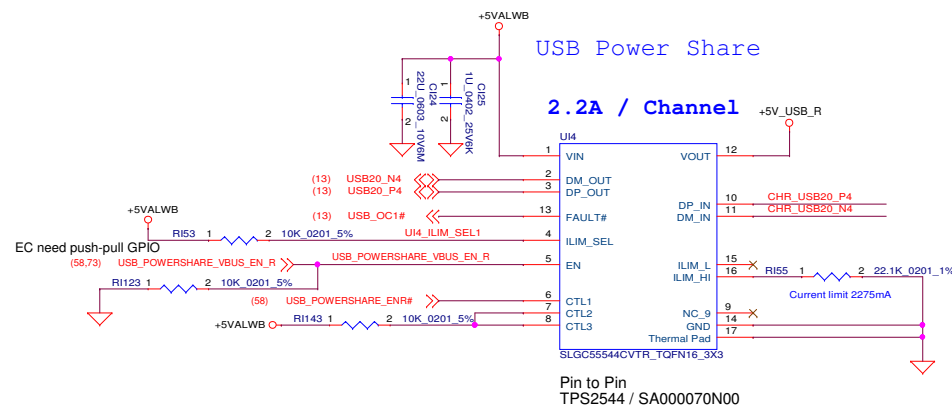




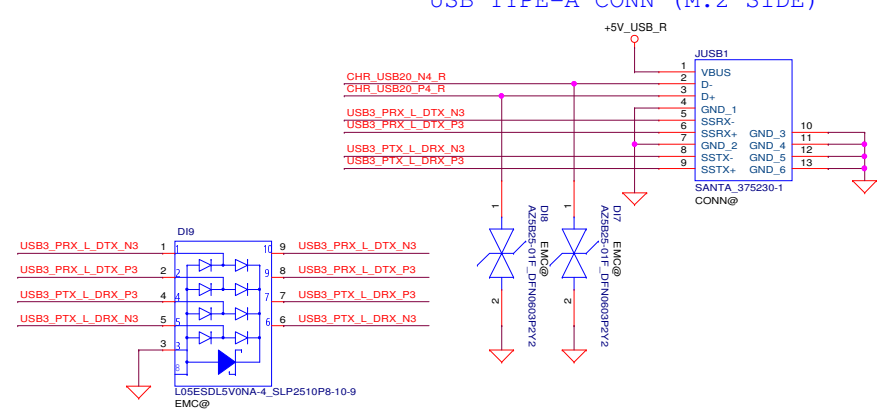
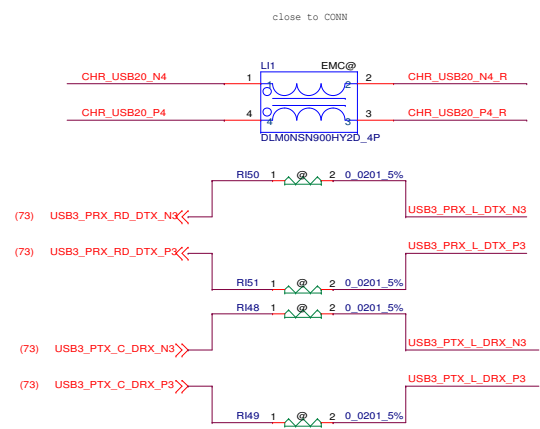
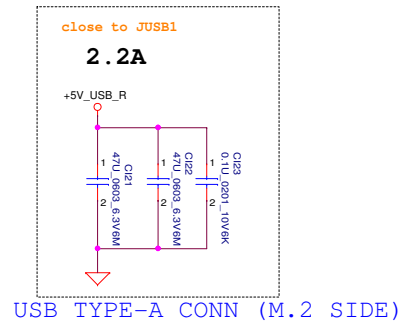
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				P069 - Reserve		
				Size	Document Number	Rev
				LA-G441P		0.1(X00)
				Date:	Friday, December 14, 2018	Sheet 69 of 100

Check done by vendor on 0321

USB Type-A Connector (M.2 SIDE)

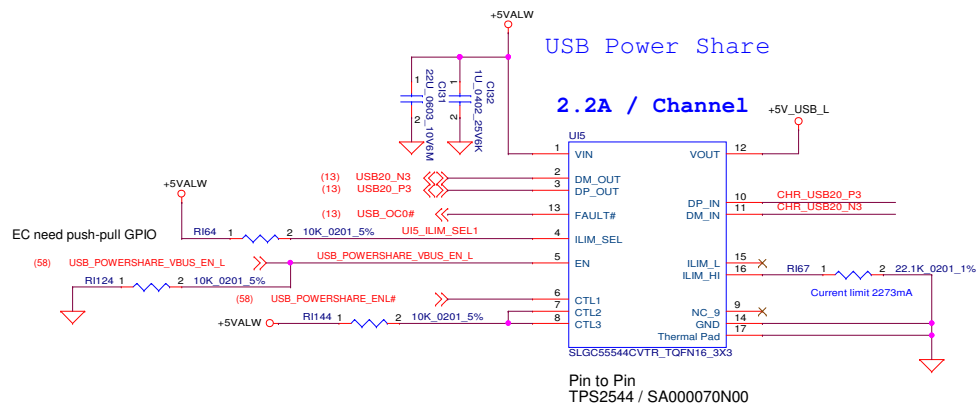


CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDP
1	1	1	1	CDP

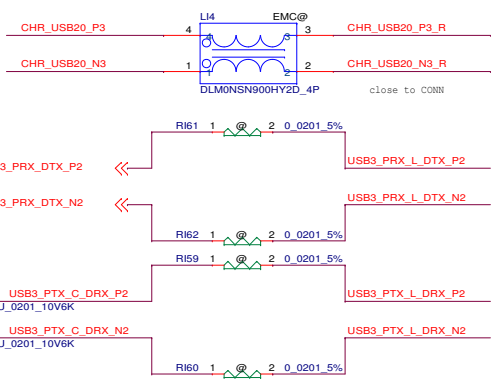
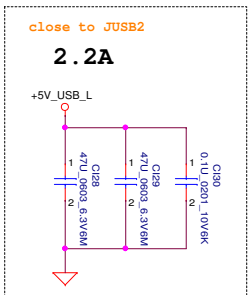


Check done by vendor on 0321

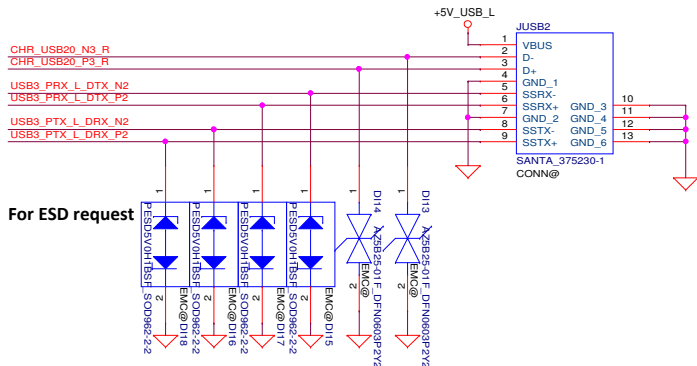
USB Type-A Connector (CPU Side)



CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDP
1	1	1	1	CDP

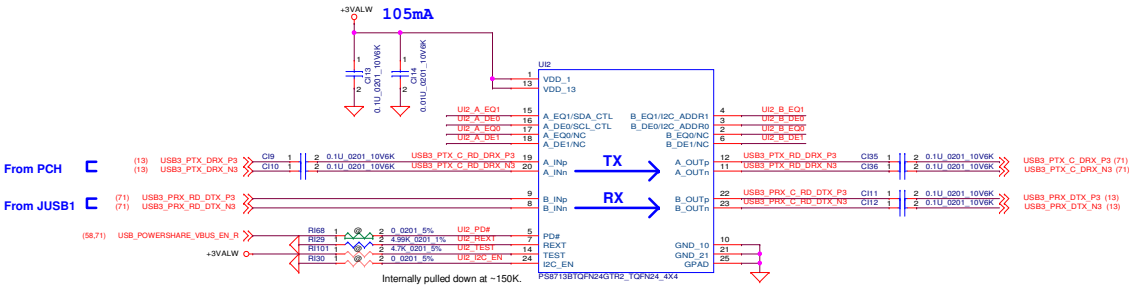


USB TYPE-A CONN (CPU SIDE)



Check done by vendor on 0309

USB3.0 Re-driver PS8713 (M.2 SIDE TO JUSB1)

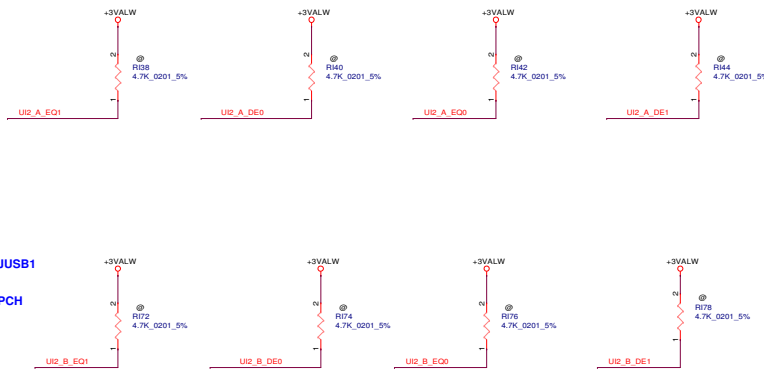


Parade_PS8713B

A_EQ1	A_EQ0	B_EQ1	B_EQ0	Recommended EQ	A_DE1	A_DE0	B_DE1	B_DE0	Recommended DE
0	0	0	0	loss up to 9.5dB	0	0	0	0	3.5dB de-emphasis
0	1	0	1	loss up to 13dB	0	1	0	1	No de-emphasis
1	0	1	0	loss up to 4.5dB	1	0	1	0	2.7dB de-emphasis
1	1	1	1	loss up to 7.5dB	1	1	1	1	5dB de-emphasis

Both A_EQ0&B_EQ have internal pull-down 150k

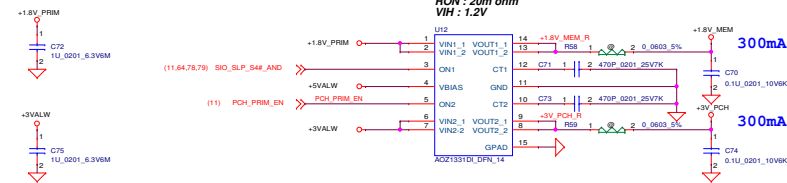
Both A_DE0&B_DE have internal pull-down 150k





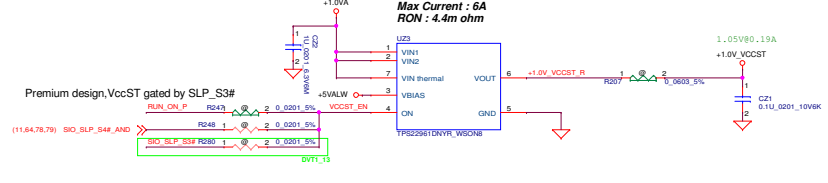
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				P074 - Reserve	
				Size	Document Number
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+3V_PCH & 1.8VU



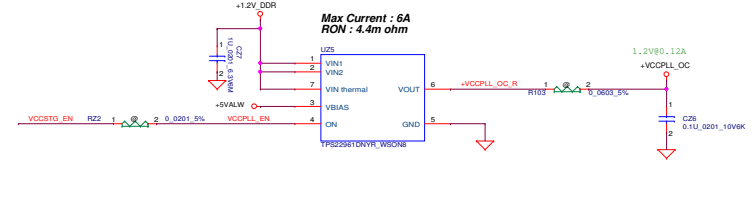
C _{IN} (µF)	Rise Time (µs) 10%-90%, C _L =0.1µF, C _{IN} =1µF, R _{DS(on)} =100Ω Typical Values at 25°C, 25V K78 10% Ceramic Cap.
0	85 68 49 45 40 37 34
220	431 297 172 147 122 106 89
470	888 583 332 269 218 189 161
1000	1700 1100 657 550 446 390 319
2200	3005 2334 1347 1152 966 867 701
4700	6053 5255 1997 2578 2101 1838 1483
10000	18330 12050 5045 5545 4155 4155 3329

+1.0V_VCCST source

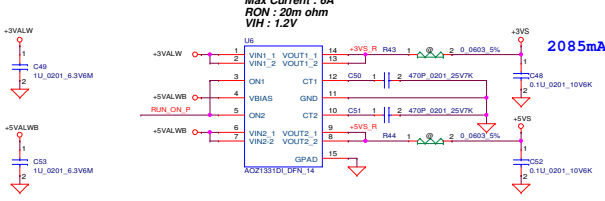


C _L (µF)	Rise Time (µs) 10%-90%, C _L =0.1µF, C _{IN} =1µF, R _{DS(on)} =100Ω Typical Values at 25°C, 25V K78 10% Ceramic Cap.
0	85 68 49 45 40 37 34
220	431 297 172 147 122 106 89
470	888 583 332 269 218 189 161
1000	1700 1100 657 550 446 390 319
2200	3005 2334 1347 1152 966 867 701
4700	6053 5255 1997 2578 2101 1838 1483
10000	18330 12050 5045 5545 4155 4155 3329

+VCCPLL_OC source

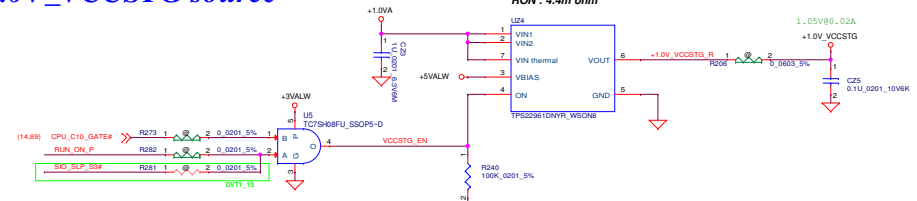


5VS & 3VS

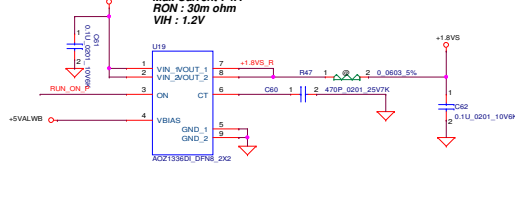


CT	Rise Time (µs) 10%-90%, C _L =0.1µF, C _{IN} =1µF, R _{DS(on)} =100Ω Typical Values at 25°C, 25V K78 10% Ceramic Cap.
0	85 68 49 45 40 37 34
220	431 297 172 147 122 106 89
470	888 583 332 269 218 189 161
1000	1700 1100 657 550 446 390 319
2200	3005 2334 1347 1152 966 867 701
4700	6053 5255 1997 2578 2101 1838 1483
10000	18330 12050 5045 5545 4155 4155 3329

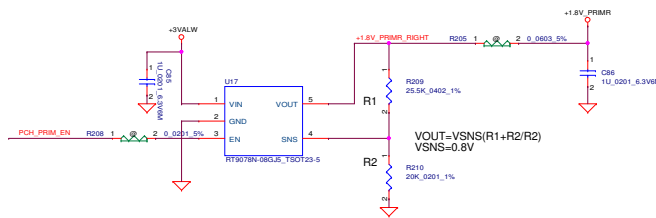
+1.0V_VCCSTG source



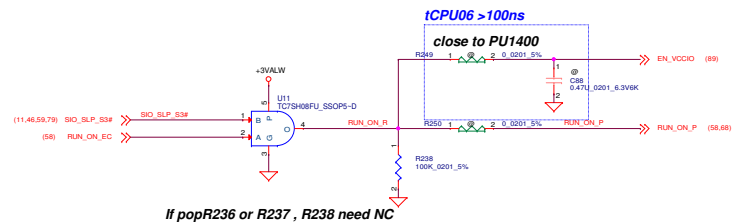
1.8VS



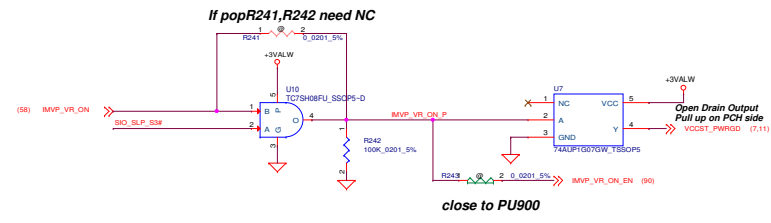
+1.8V_PRIMR(Right side) LDO



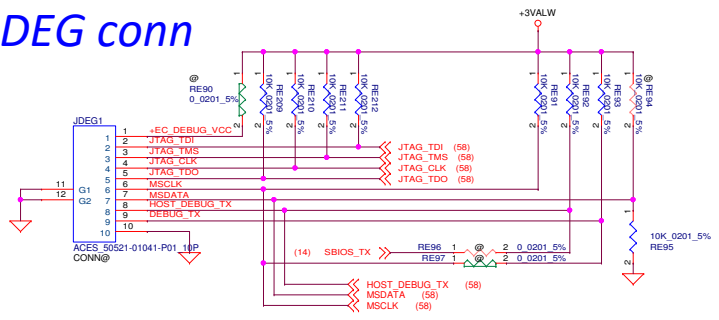
RUN_ON(VS EN)



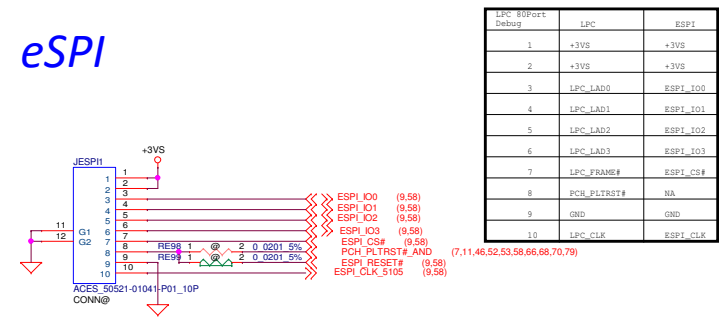
IMVP_VR_ON & VCCST_PWRGD



DEG conn

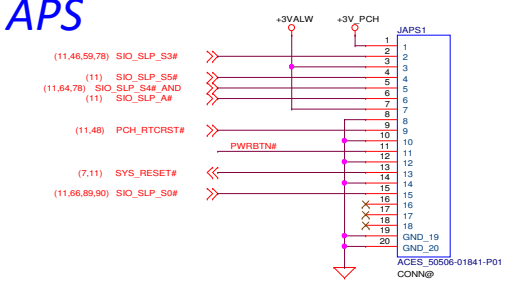


eSPI

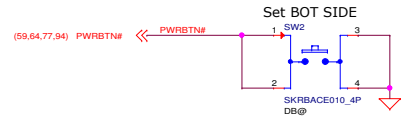


LPC Support Debug	LPC	eSPI
1	+3VS	+3VS
2	+3VS	+3VS
3	LPC_LAD0	eSPI_IO0
4	LPC_LAD1	eSPI_IO1
5	LPC_LAD2	eSPI_IO2
6	LPC_LAD3	eSPI_IO3
7	LPC_FRAME#	eSPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLK	eSPI_CLK

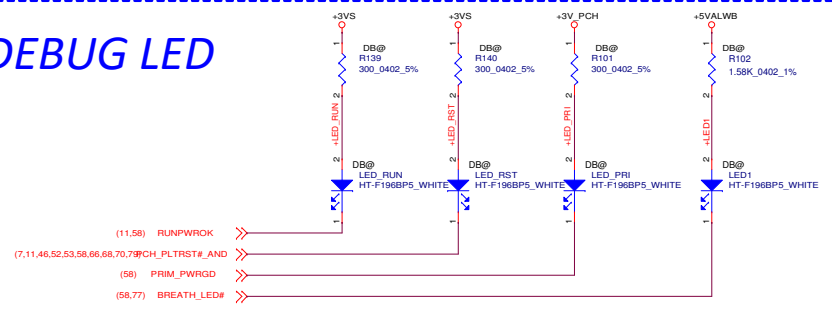
APS

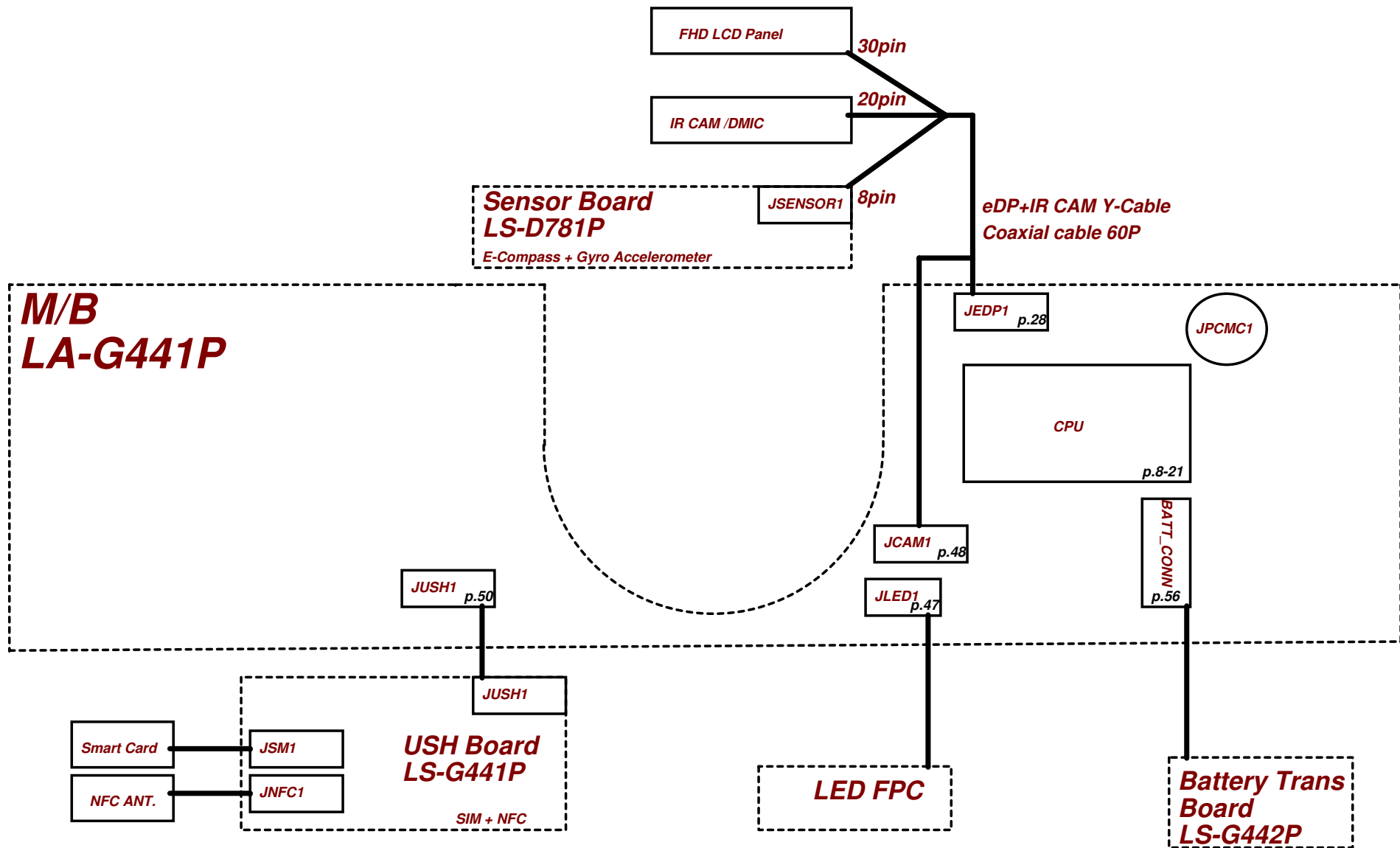


Test Power Button

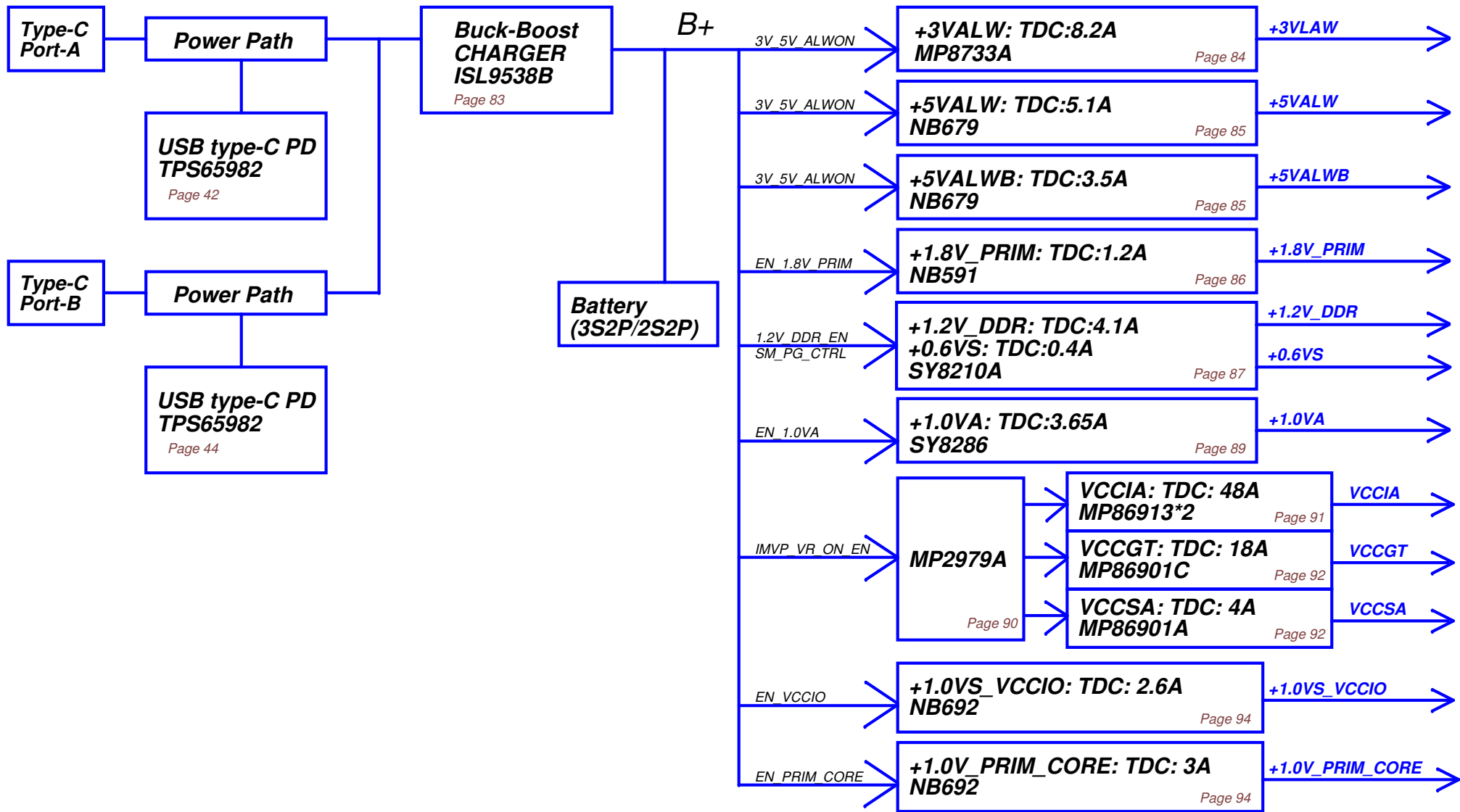


DEBUG LED



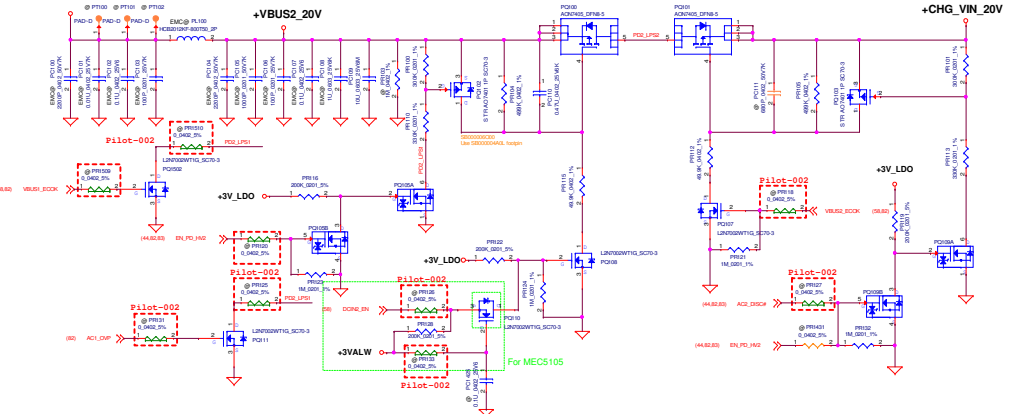


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										P080 - DaughterB Block Diagram	
										Document Number	
										LA-G441P	
										Date: Friday, December 14, 2018	
										Sheet 80 of 100	

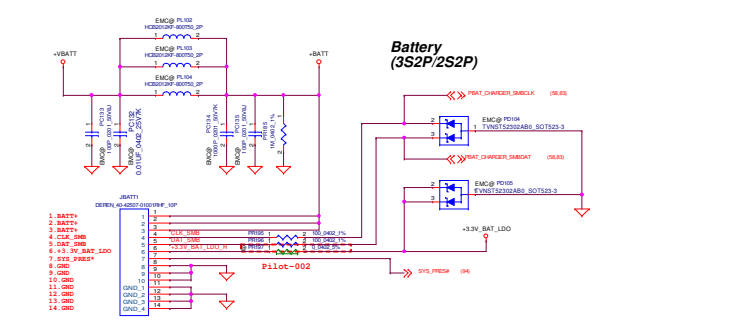
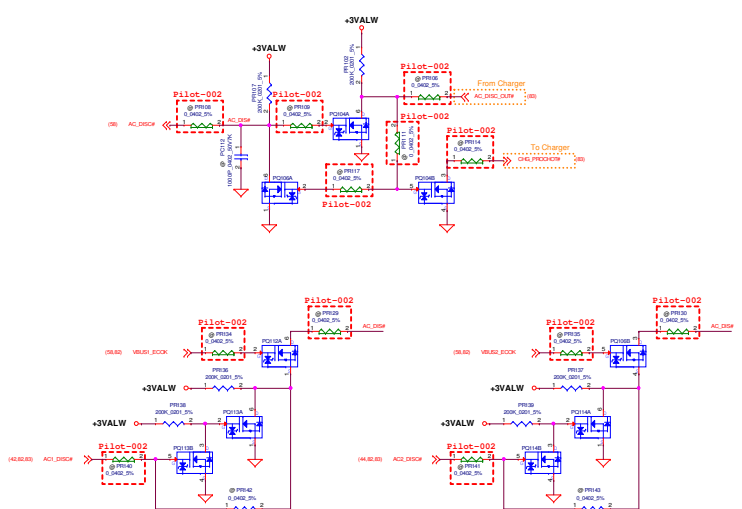
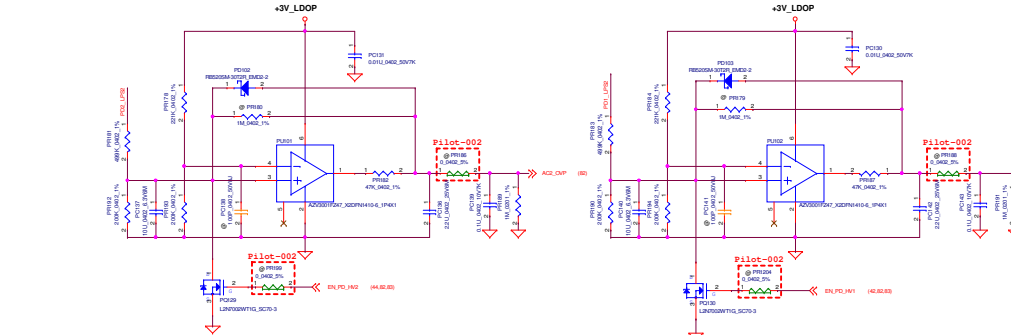
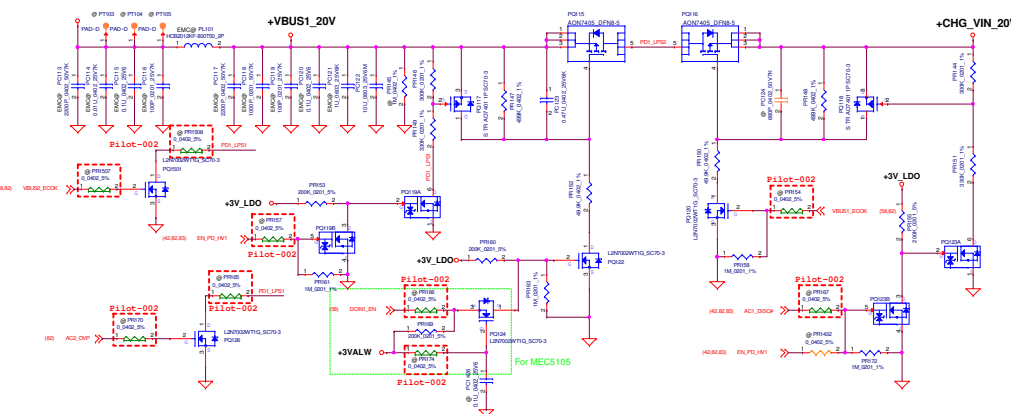


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					LA-F371P	0.1
				Date:	Friday, December 14, 2018	Sheet 81 of 100

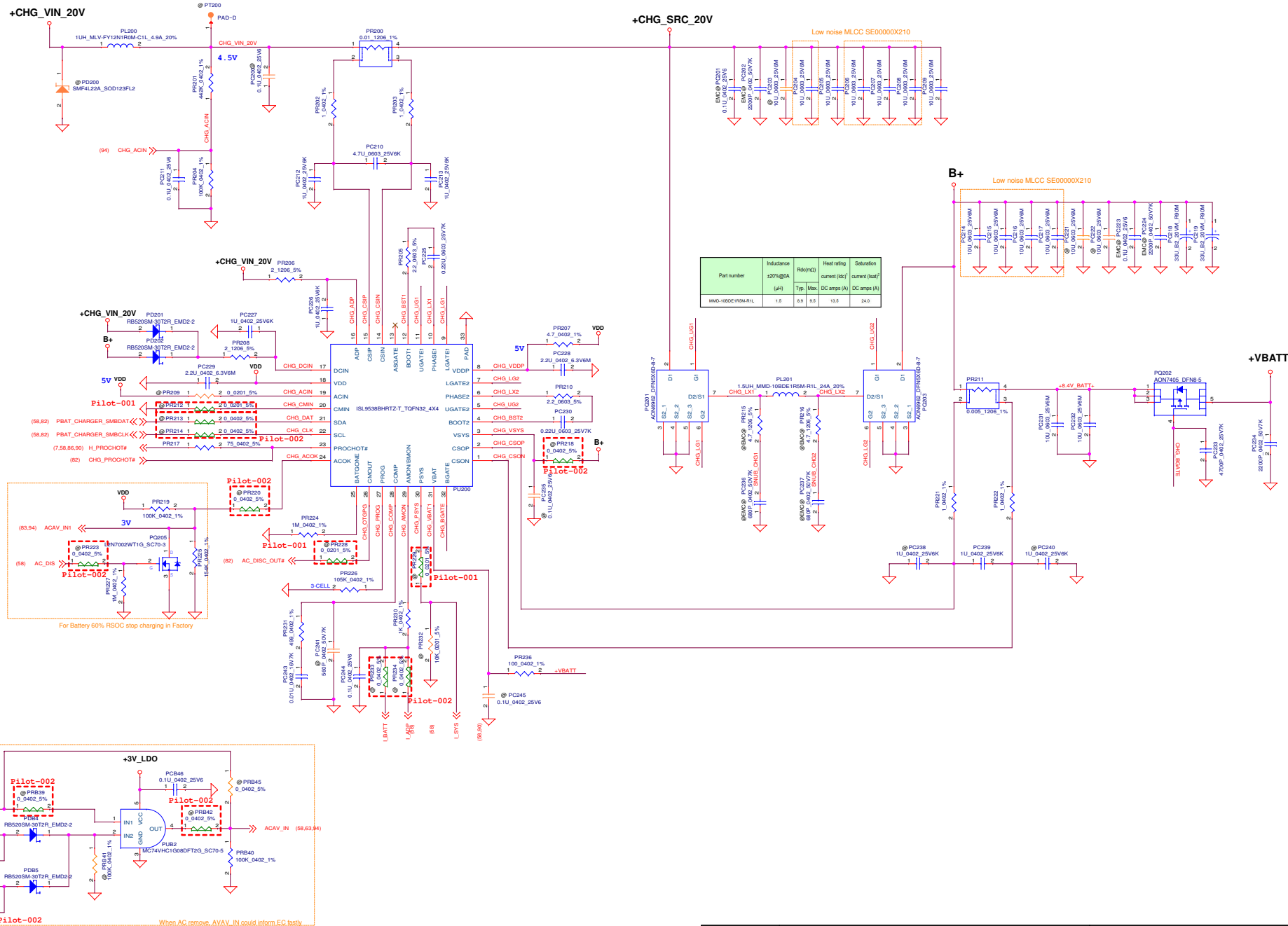
Type C adapter input_2
+TBT_VBUS2



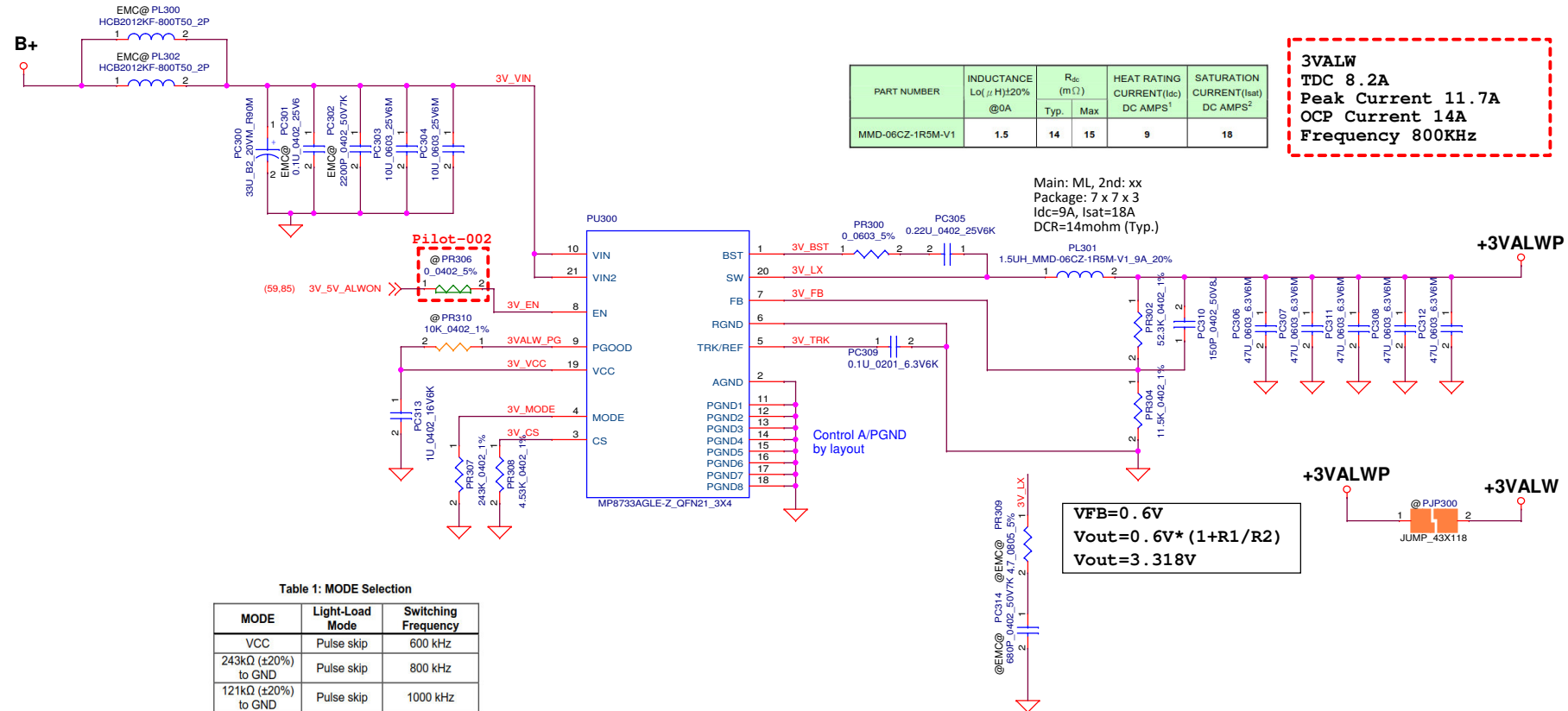
Type C adapter input_1
+TBT_VBUS1



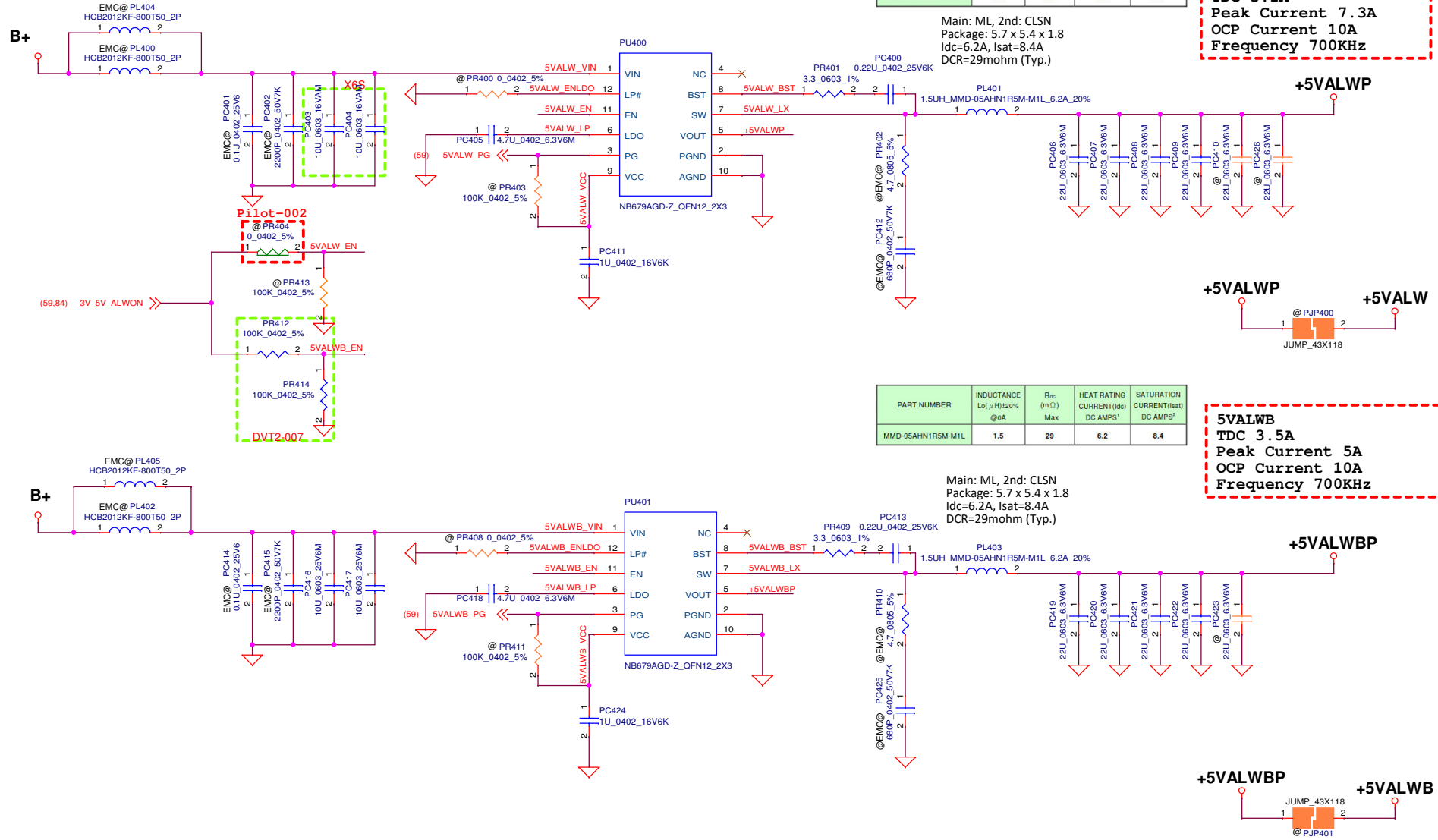
Charger controller(40.1), Support component(40.2)



3V controller(35.1), Support component(35.2)

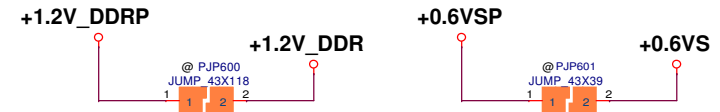
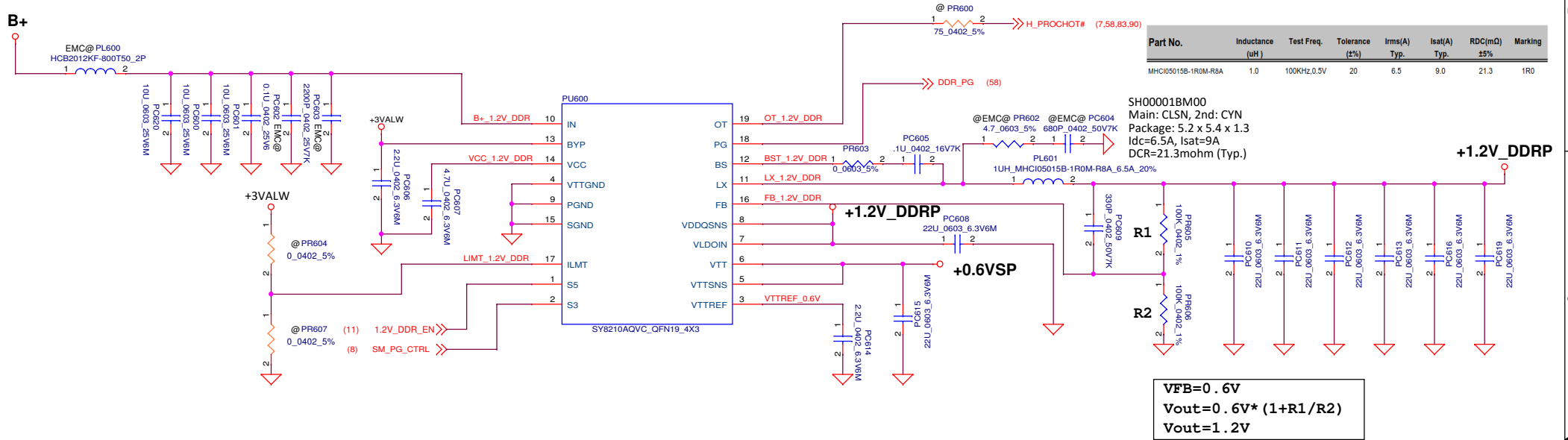


5V controller(35.1), Support component(35.2)



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DDR controller(35.3), Support component(35.4)



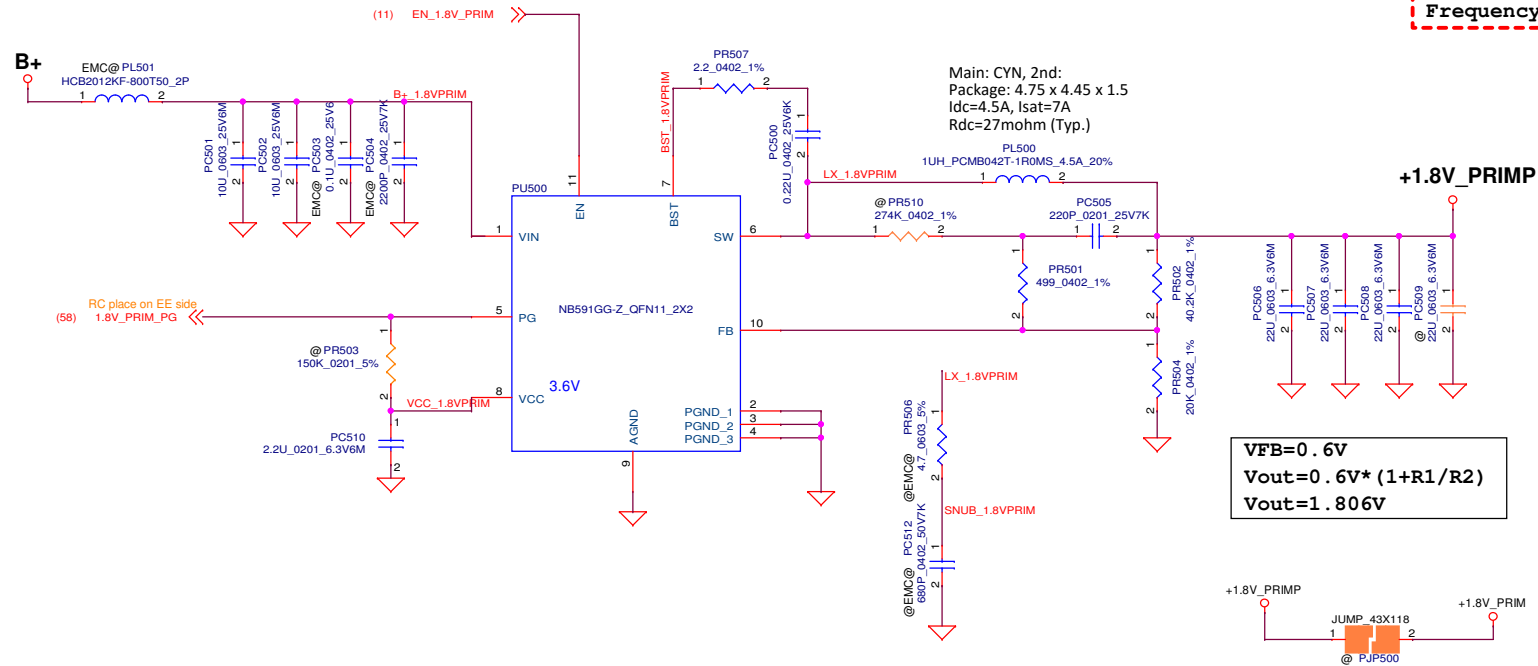
+1.2V_DDR
TDC 4.1A
Peak Current 5.8A
OCP Current 12A
Frequency 600KHz

+0.6VS
TDC 0.4A
Peak Current 0.6A
OCP Current 2A (fix)
Frequency 600KHz

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Size	Document Number	Rev		0.1	
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+1.8V_PRIM controller(35.13), Support component(35.14)

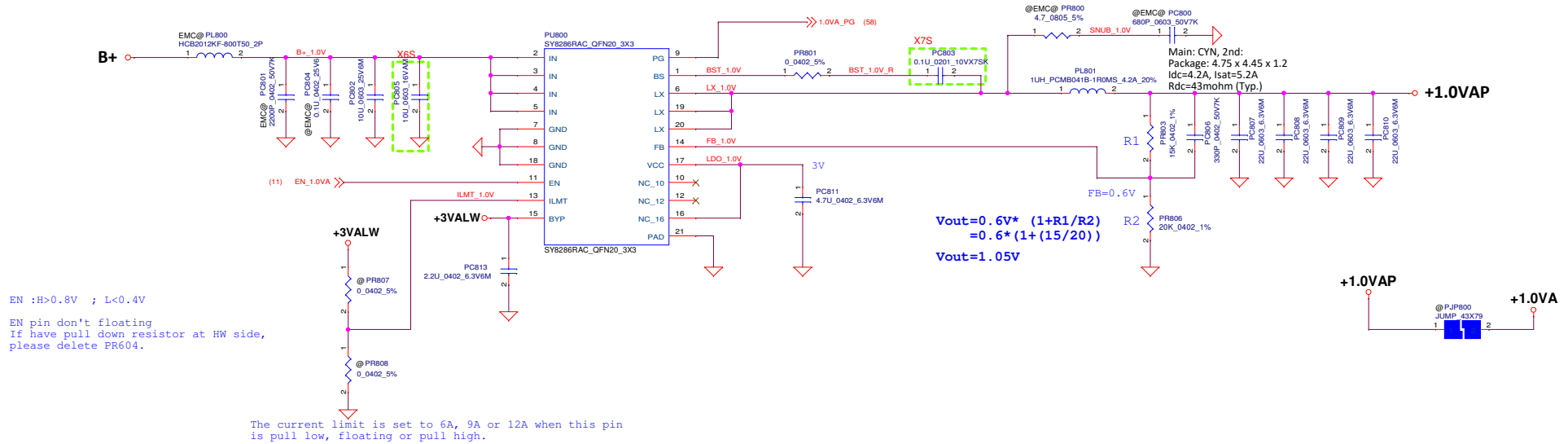
1.8V_PRIM
TDC 1.2
Peak Current 1.6A
OCP 4A (Typ.)
Frequency 750KHz



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1.05V controller(35.5), Support component(35.6)

```
+1.0VA
TDC 3.65A
Peak Current 5.2A
OCP current 9.0A
Frequency 500KHz
```

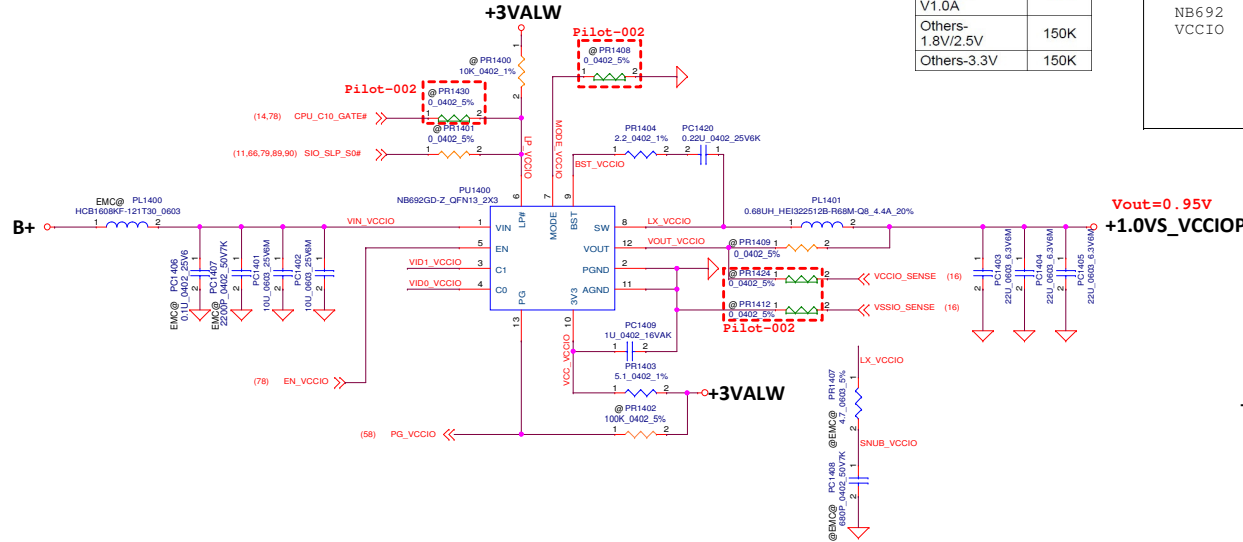
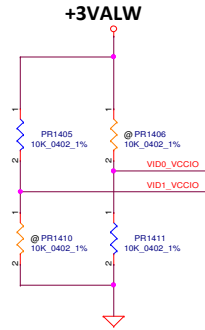


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					LA-E671P	1.0
Date:	Friday, December 14, 2016			Sheet	88	of 100

VCCIO controller(35.37), Support component(35.38)

V _{OUT} (V)	R _{MODE} (Ω)
VCCIO	0
PRIMCORE	Float
EDRAM/ EOPIO/ V1.0A	100K
Others- 1.8V/2.5V	150K
Others-3.3V	150K

	LPM	VID1	VID0	Vout
NB692 VCCIO	0	X	X	0 (LPM)
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

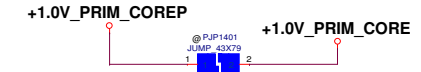
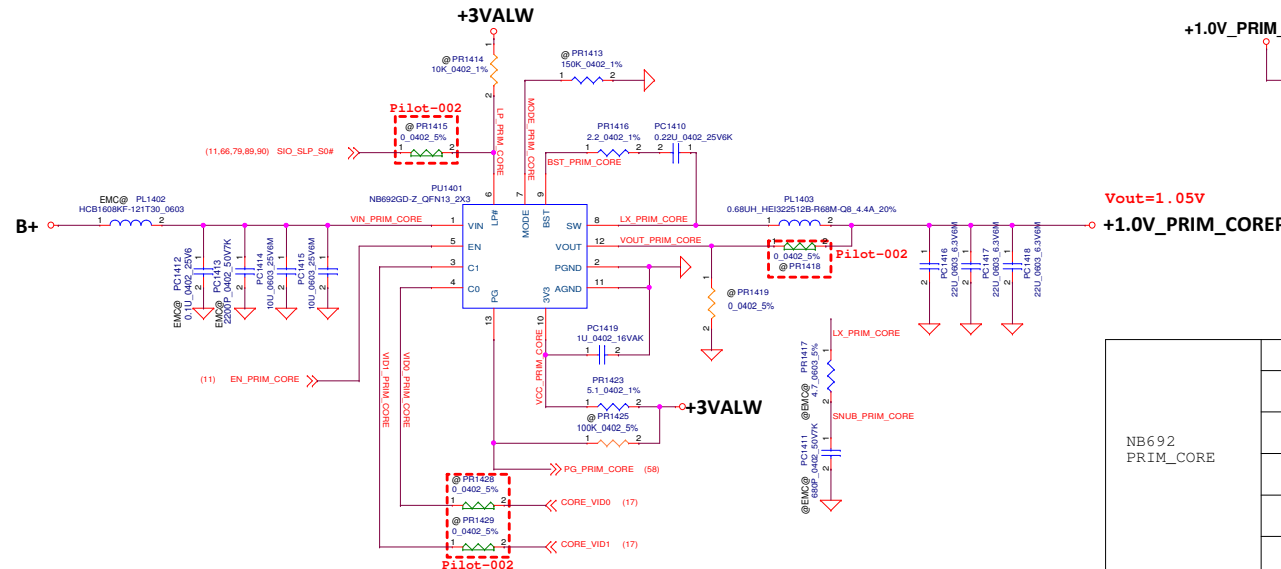
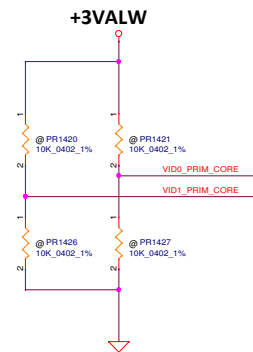


VCCIO
TDC 2.6A
Peak Current 3.7 A
OCP Current 7.6 A Fix by IC
MIN:7A
MAX:8.5A
Frequency:750KHz



PRIM_CORE
TDC 3A
Peak Current 4.3 A
OCP Current 7.6 A Fix by IC
MIN:7A
MAX:8.5A
Frequency:750KHz

+1.0V_PROM controller(35.35), Support component(35.36)



Vout=1.05V
+1.0V_PRIM_COREP

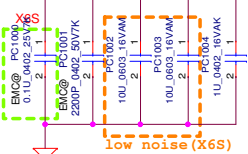
	LPM	VID1	VID0	Vout
NB692 PRIM_CORE	0	X	X	0.75 (LPM)
	1	0	0	0.9
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05

+1.0VS_VCCIO controller(35.21), Support component(35.22)
+1.0V_PRIM_CORE controller(35.23), Support component(35.24)

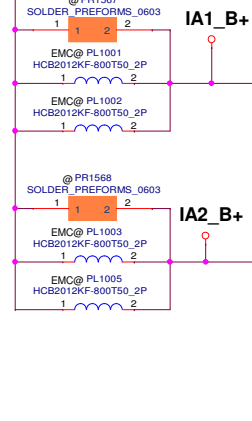
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VCC_CORE Dr. MOS (36.2), Support component(36.3)

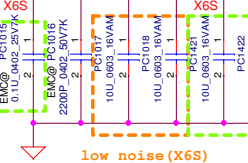
IA1_B+



B+



IA2_B+



+3VALW

Pilot-002

@PR1000 0.0402_5%

PC1005 0.22u_0402_25VAK

1u_0402_16VAK

X6S

VCC_CORE1

AGND

BST

PC1006 0.22u_0402_25VAK

1u_0402_16VAK

X6S

BST_CORE1

PC1007 0.22u_0402_25VAK

1u_0402_16VAK

X6S

BST_CORE1

PC1008 0.22u_0402_25VAK

1u_0402_16VAK

X6S

BST_CORE1

PC1009 0.22u_0402_25VAK

1u_0402_16VAK

X6S

BST_CORE1

PC1010 0.22u_0402_25VAK

1u_0402_16VAK

X6S

BST_CORE1

PC1011 0.22u_0402_25VAK

1u_0402_16VAK

X6S

BST_CORE1

PC1012 0.22u_0402_25VAK

1u_0402_16VAK

X6S

BST_CORE1

PC1013 0.22u_0402_25VAK

1u_0402_16VAK

X6S

BST_CORE1

PC1014 0.22u_0402_25VAK

1u_0402_16VAK

X6S

BST_CORE1

PC1015 0.22u_0402_25VAK

1u_0402_16VAK

X6S

BST_CORE1

PC1016 0.22u_0402_25VAK

1u_0402_16VAK

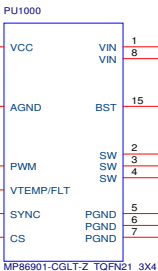
X6S

BST_CORE1

PC1017 0.22u_0402_25VAK

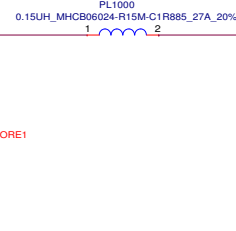
1u_0402_16VAK

X6S



Main: CLSN, 2nd:
Package: 7.5 x 6.9 x 2.4
Idc=27A, Isat=42A
Rdc=0.88mohm +/-5%

+VCC_CORE



+3VALW

Pilot-002

@PR1000 0.0402_5%

PC1020 0.22u_0402_25VAK

1u_0402_16VAK

X6S

VCC_CORE2

AGND

BST

PC1021 0.22u_0402_25VAK

1u_0402_16VAK

X6S

BST_CORE2

PC1022 0.22u_0402_25VAK

1u_0402_16VAK

X6S

BST_CORE2

PC1023 0.22u_0402_25VAK

1u_0402_16VAK

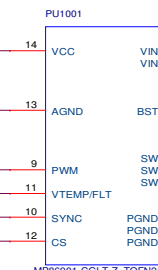
X6S

BST_CORE2

PC1024 0.22u_0402_25VAK

1u_0402_16VAK

X6S



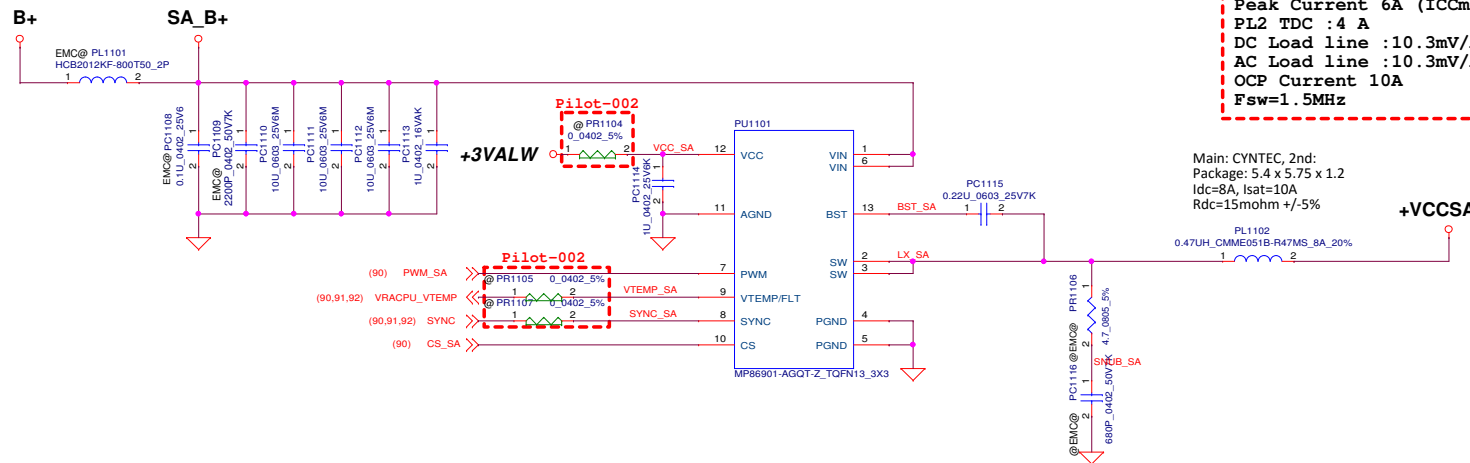
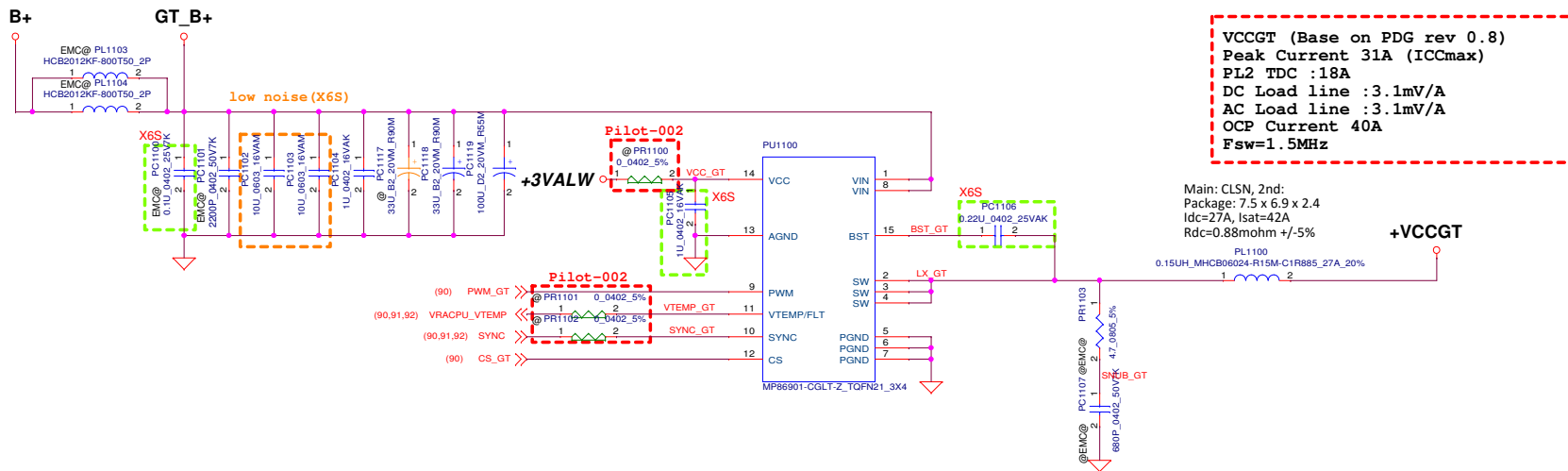
Main: CLSN, 2nd:
Package: 7.5 x 6.9 x 2.4
Idc=27A, Isat=42A
Rdc=0.88mohm +/-5%

+VCC_CORE



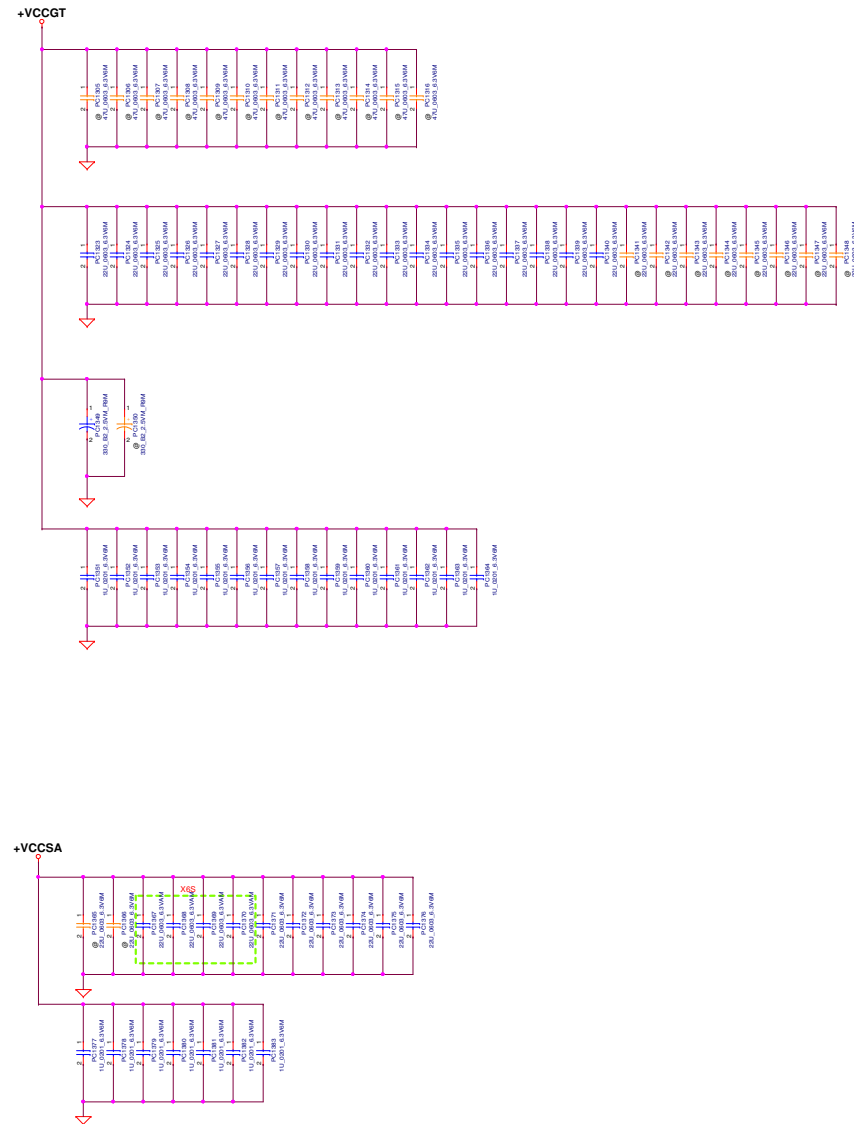
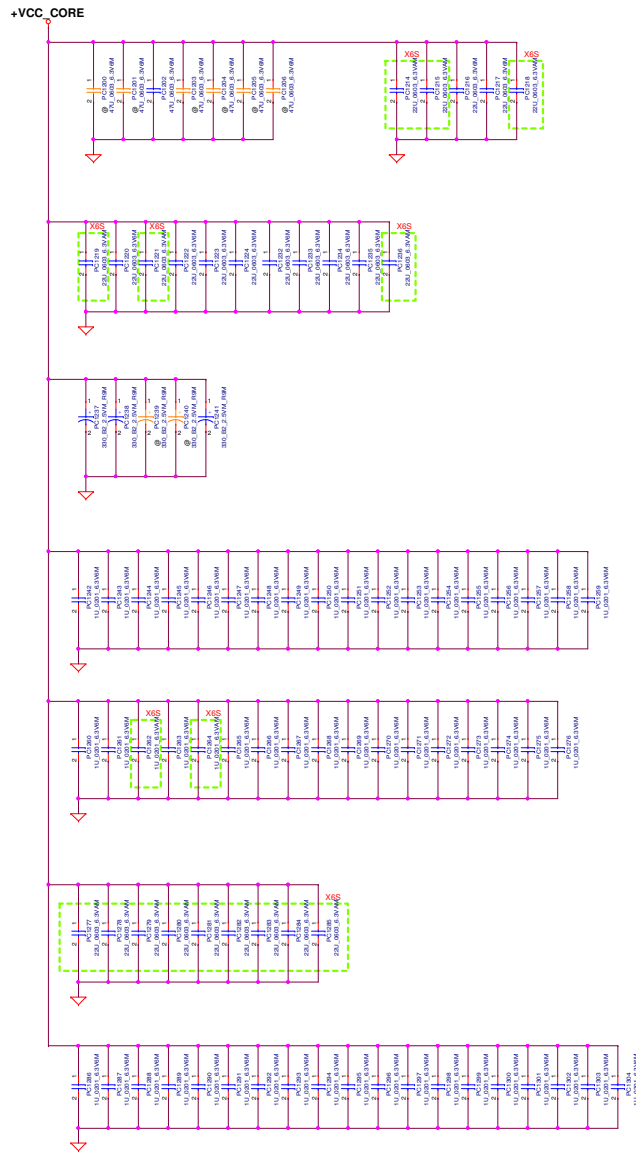
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					LA-F371P	0.1
				Date:	Friday, December 14, 2018	Sheet 91 of 100

VCC_GT/SA Dr. MOS (36.2), Support component(36.3)



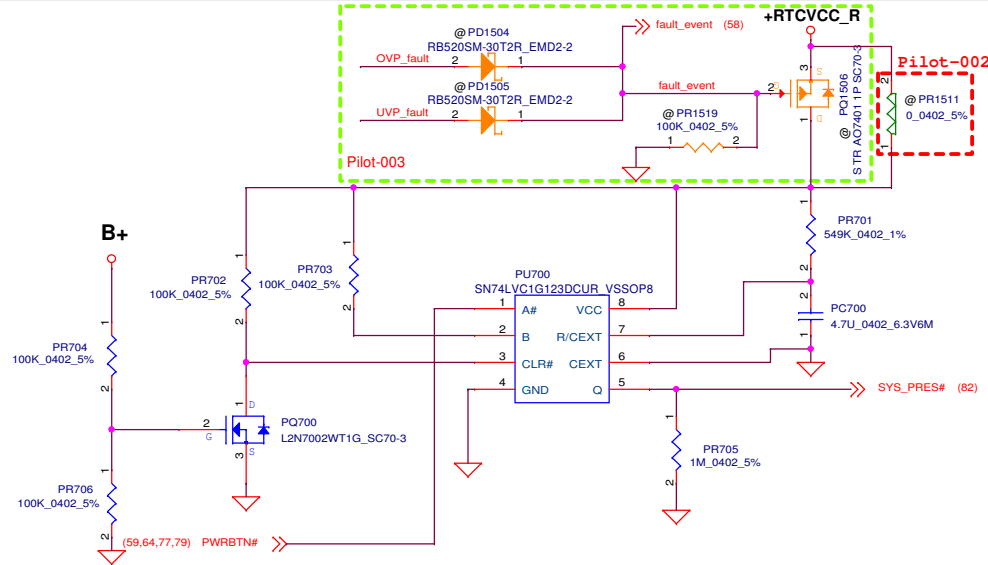
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				Date:	Friday, December 14, 2018	Sheet 92 of 100

VCC_Core Output Cap(36.4), VCCGT Output Cap(36.5), VCCSA Output Cap(36.6)



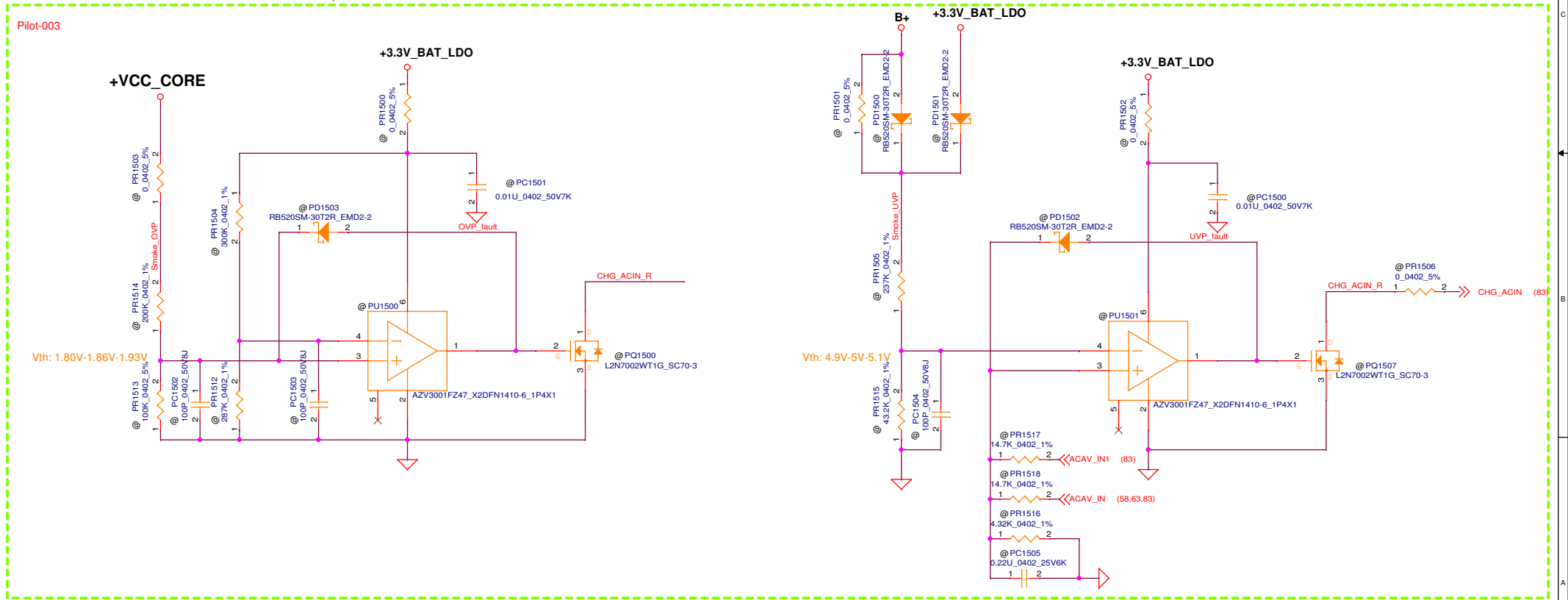
VCC_CORE output cap(36.4), VCC_GT output cap(36.5), VCC_SA output cap(36.6)

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1.0		1.0		1.0	
Date		Friday, December 19, 2013		Sheet	
30		of		100	



FUNCTION TABLE

INPUTS			OUTPUTS Q
CLR	\bar{A}	B	
L	X	X	L
X	H	X	L ⁽¹⁾
X	X	L	L ⁽¹⁾
H	L	↑	
H	↓	H	
↑	L	H	





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